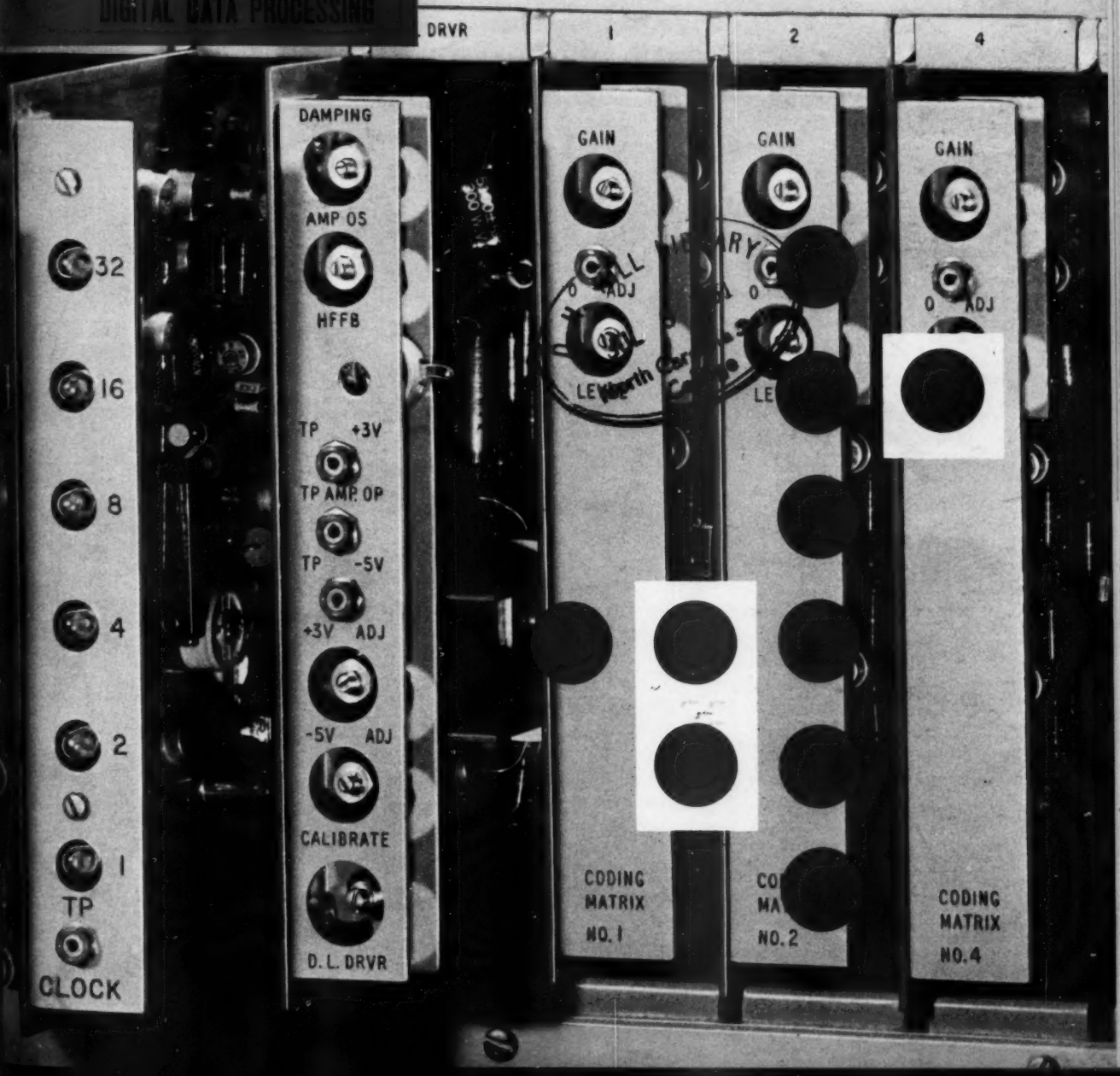
ELECTRONIC PROGRESS

RAYTHEON

MARCH-APRIL 1961

in this issue:

DIGITAL DATA PROCESSING



VOLUME V MARCH - APRIL 1961 NUMBER 6

ELECTRONIC PROGRESS

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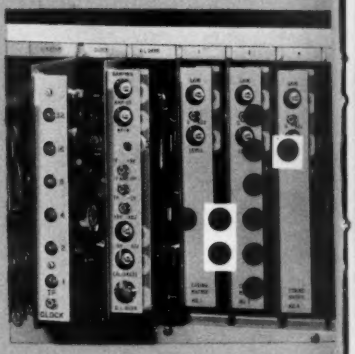

Raytheon's Analog-to-Digital Converter synthesizes many of the advances that modern data processing equipment offers —ultra-high speed, modular construction, multiple applications. Some of these aspects of digital data processing are discussed in this issue.

about this issue . . .

In the Spring of 1960, Raytheon established in its Equipment Division a new unit, the Communications and Data Processing Operation (CADPO). This action represented the formal grouping of many of the Company's elements concerned with study and development related to data processing and communications. To acquaint the reader with the scope of the data processing activity, the editors have chosen for this issue five articles written by members of the Operation's staff.

In its first year, CADPO has achieved some noteworthy objectives. Equipment developed includes: a 5 Mc analog-to-digital converter; digital equipment for a 96-channel pulse coded modulation system; a complete line of 1 Mc transistorized digital building blocks; an extremely high-speed analog-to-digital converter for the Pincushion ICBM tracking radar; and the Cybertron, a self-organizing data processor with learning ability. The data processing group has, in recent months, made significant contributions to several large systems studies for military customers.

The complexity of modern electronics systems often demands the skillful application of data processing techniques. It is hoped that this issue will encourage our systems groups to utilize the data processing talents that CADPO has to offer.

MARTIN SCHILLING
Vice President
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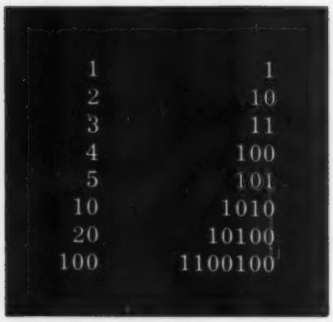
DEFINITION: *Digital data processing is an efficient manipulation of information by means of a digitally coded numerical sequence .... usually based on the binary number system.*



DIGITAL DATA PROCESSING... AN INTRODUCTION

by Seymour Greenfield , Rolf Kates and Herbert S. Sobel

DDP

Introduction

IN RECENT YEARS the size and complexity of electronic systems, both military and commercial, has increased drastically. Communications equipment has become merely a small part of large weapon systems, and radar equipment has often been incorporated as subsystems within large integrated systems. As the complexity of these systems has increased, so has the amount of information which is handled. The use of inherently faster techniques for processing large quantities of data has become necessary. This has resulted in the rapid development of the technique of digital data processing (DDP). Engineers working on electronic systems are thus forced into greater awareness of the effect of digital data processing upon their individual engineering specialties, as well as upon the over-all system of which they are a part.

There are two fundamental families of machines which are commonly used for digital data processing. These are: a) the general purpose computer, and b) the special purpose computer or data processor which is the machine of primary interest in this article.

The general purpose computer is a device primarily designed to perform many different types of computation and data storing operations. It can be instructed to perform one or many applications quite readily. On the other hand, a special purpose machine, which is not necessarily a calculating device, cannot readily be instructed to perform many different tasks. It has a fixed purpose and contains a fixed program or set of instructions which cannot be altered. Thus, the general purpose machine is a flexible device which can be used for many applications simultaneously whereas the special purpose machine is an inflexible device which can perform only one or at most a few applications in each machine.

Quite often it is uneconomical to use a general purpose computer for a specific job because the full capabilities of the device cannot be utilized. In many cases, the general purpose computer cannot efficiently perform the required processing. In these instances, a special purpose data processor is required.

In this paper the machine of interest is the special purpose machine, which is hereafter referred to as a digital data processor (DDP). Its main purpose is often to sort data and perform logical decisions, with a secondary purpose of performing computation associated with the decision process. Because the system example to be discussed suggests that a DDP may be linked to a general purpose computer, the use of the word computer shall imply general purpose design.

Structure of a Typical Data Processor

The model of Figure 1 is a general representation of many of the commonly encountered data processors. Its particular configuration depends primarily on its input source and the desired output function. The mode of operation of digital equipment can be in either real or non-real time. The real-time system processes inputs as they arrive, usually in a manner such that the processed data is capable of modifying the input information as it arrives. This modification is indicated by the feedback loop to the input in the model of Figure 1. This may be an indirect modification, as in a search radar system in which the processed radar data may be responsible for the launching of retaliatory missiles. Non-real time processing is such that the data resulting from the occurrence of an event is stored for later handling by a data processor. The storage media may be magnetic tape, magnetic core planes, or magnetic drum.

Description of a Generalized Model

Figure 1 shows an input, either analog or digital in nature, which must be converted to the digital language of the particular data processor.* The nature of the input source may be radar pulses, radio frequency, or stored digital data. The digitized input is then sorted and stored, not necessarily in that sequence. Often the information is sorted as it is placed into storage, thus combining the two operations.

The stored information is available for the decision-making process. The types of decisions may be of a categorizing or arithmetic nature, or combinations of both. The number of decisions to be made usually depends upon the mode of operation of the data processor. In a real-time mode, processing must be performed while information is entering the system, so that the digital rate of the data processor is compatible with the input information arrival rate. Thus, all decision processes must be made before the input storage device is overloaded, or else risk the loss of desired data.

The presentation of the digitized output can be made in many alternate ways. If the data is being preprocessed by the DDP for further calculations, then the data must be presented to an external general purpose computer, and must be rearranged so that it is in the digital language of the computer. This new arrangement is known as the "format." It is not uncommon to present the output to a communications link to be sent to some centralized location, often the control center of a system. If the data processor is part of a digital control system, then the output is used to modify the input via a feedback loop. In many instances the output is displayed (visually or audibly) immediately after the decision process, possibly by use of a digital-to-analog converter.

The placement of the digital data processor within an over-all system determines a further classification of the system into either the centralized† or decentralized type.

*This is covered in detail in "Analog to Digital Converter Techniques" by C. F. Crocker elsewhere in this issue.

†An application of this is given in the article "Centralized Data Processing" by E. L. Gilfix.

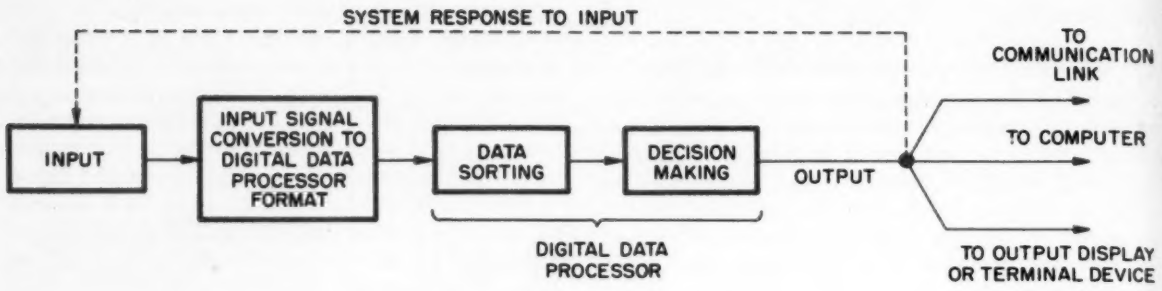


Figure 1. Generalized model of data processing system

A decentralized data processing system functions by means of units located at each input source. An example of this is an artillery fire control data processor, where a digital device oversees the tracking and target prediction of its assigned weapon. Many radar data processors and chemical processes are also typical examples of decentralized systems.

Although a large portion of the data processing done today is of the decentralized type, the centralized processing method is coming more to the forefront as the basis of military digital communications systems. Massive information is accepted at a centralized control station from inputs at various remote locations. A great deal of duplication of processing at each source is thus eliminated.

The Radar Case: A Data Processing Application

The processing of radar returns with digital data processing techniques is fast becoming an accepted procedure. The high speed of incoming target data in many modern pulsed radars often makes the use of visual observers impossible. The inherent speed limitations of analog processing has further necessitated digital electronics. Most important of all is the fact that input radar data, with an order of magnitude of millions of pulses per second, must go through numerous calculations in real time by a general purpose computer. Since the computer accepts data at a rate of only hundreds of bits per second, buffering is necessary to sort out unnecessary data and perform a variety of decision processes. A digital data processor is inserted between the radar and the general purpose computer to perform this complex buffering and produce the required compatibility. The generalized data processor of Figure 1 applies as a model for the buffering performed on incoming radar data.

Using the radar case as a systems example of digital data processing, the functions of the radar can be classified according to the type of operation performed; e.g., either search or tracking. To further narrow the scope of the example, the case of the search radar only is considered. Since the radar's primary function is target detection, information for decision making must be presented. This information is also used for target position estimation which is a necessary characteristic in order to distinquish between new and old targets.

The search radar can be classified by either of two functions: Alarm or early warning, and acquisition. From the data processing viewpoint, the alarm radar is a sorting and target decision device which indicates the presence of a target. The acquisition radar, however, requires the data processor to supply more thorough decisions on target position so that this information can be passed on to a tracking system. Thus, the data processor for the acquisition case has greater complexity. In both cases, a large number of targets must be handled simultaneously, requiring a large amount of digital storage.

Figure 2 shows the functioning of a typical search radar data processor. For its operation, radar echoes from the receiver are passed on to the DDP, which quantizes the signal into the desired digital levels, sorts the radar parameters in a digital memory, and then performs two decision processes:

1. A decision on the validity of target information. This is the target detection process in which valid targets are to be accepted and false targets (caused by noise or other disturbances) rejected.
2. A determination of target position parameters, such as azimuth, range, and range rate. In this manner information is not only processed but also condensed.

If the radar is at a remote site, the output information is sent via communication link to a central location. It may also be sent to a terminal device at the radar site.

In the case of an acquisition system, a computer (external to the DDP) usually calculates target trajectory based on information obtained from the data processor. This data is used to initiate the operation of a tracking radar which locks onto the target. Thus the DDP is linked to an input radar source, a computer, and a tracking system containing another radar and a tracking data processor.

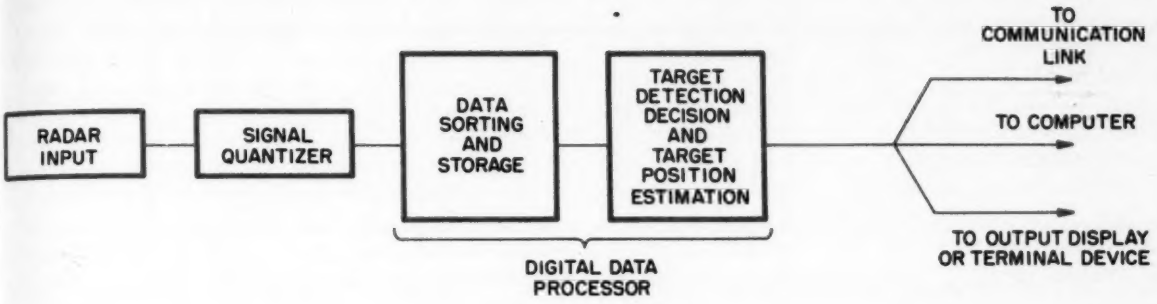


Figure 2. Typical search radar data processor

The Basic Tools of Data Processing

A system such as that in Figure 2 requires for its implementation three specific data processing tools:

1. The language used by the data processor,
2. The logical algebra which describes the functioning of the data processor,
3. The circuits which implement the logical algebra and thus do the actual functioning of the data processor.

The next three sections describe each of the above three items.

1. The Language

Data processing systems deal with information of various forms. The languages which are used are varied but have a certain basic similarity. Digital systems generally use a binary number system in which the radix (or base) is two as opposed to the more familar decimal number system, in which the radix is ten. Both number systems are positional in that the value of the number is a function of digit position.

For example, the decimal number 210 can be expressed as the sum of a series of powers of the radix *ten*. Thus

$$(210)_{\text{base }10} = 2 \times 10^2 + 1 \times 10^1 + 0 \times 10^0.$$

In general, it is possible to express any decimal number by means of a power series with an integer radix. Thus, a decimal number N may be expressed as

$$N = b_n R^n + b_{n-1} R^{n-1} + b_{n-2} R^{n-2} + \ldots + b_0 R^0$$

or in closed form as

$$N = \sum_{n=m}^{o} b_n R_n \quad ,$$

where m is an integer and is equal to one less than the total number of positions in the radix number considered.

For example, consider the binary number 1011 with a radix of two. There are four positions (m = 3) in which: $b_3 = 1$, $b_2 = 0$, $b_1 = 1$ and $b_0 = 1$. Consequently,

$$N = b_3 \times 2^3 + b_2 \times 2^2 + b_1 \times 2^1 + b_0 \times 2^0$$
$$= 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 = (11)_{\text{base }10}.$$

Table I illustrates a comparison between decimal numbers and their corresponding binary numbers.

TABLE I

Decimal Numbers	*Binary Numbers*
1	1
2	10
3	11
4	100
5	101
10	1010
20	10100
100	1100100

Often it is desirable to express fractions in a binary form. This can be accomplished in a manner similar to expressing a whole number. The decimal fraction F may be expressed as

$$F = b_{-1}R^{-1} + b_{-2}R^{-2} + b_{-3}R^{-3} + \ldots + b_{-n}R^{-n}$$

or as $$F = \sum_{n=1}^{m} b_{-n}R^{-n},$$

where m equals the total number of positions in the number.

Thus, in a straight binary system any number is represented by the appropriate use of 1's and 0's about a point. As in decimal notation, a floating-point technique may be used for the binary case.

Several variations of the straight binary system are also used. In some schemes the binary digits may be arranged to represent other number base systems. Three particular examples of this bear mention. The first of these is the base 8 system. This is referred to as octal and utilizes groups of 3 binary digits. Thus (001, 010,

$101) = (125)_{\text{base } 8} = 1 \times 8^2 + 2 \times 8^1 + 5 \times 8^0 = (85)_{\text{base } 10}$. A second common numbering is hexadecimal and utilizes groups of 4 bits in a manner similar to that described for octal. These two systems make a relatively straightforward use of the binary system. The third system (or set of systems) is a direct representation of decimal numbers.* In this case, four bits must be used to represent the ten possible digits. The weighting factor of each of the four bits varies with different methods. The most common of these is that called 8421 in which the weighting factor of each of the bits in order to the left of a point is 8, 4, 2, and 1, respectively, as described above. Thus $(0111)_{\text{base } 2} = 0 \times 8 + 1 \times 4 + 1 \times 2 + 1 \times 1 = (7)_{\text{base } 10}$. These are typical examples of languages which represent numeric information in data processing systems.

It is often desirable to represent alphabetic as well as numeric information in a system. This information is called alphanumeric and is usually represented by a sequence of bits. In typical alphanumeric languages in data processing systems, sequences of six bits are used to represent some 64 characters and punctuation symbols. The individual weight of the bits in alphanumeric languages is generally lost. Instead it is the complete six-bit sequence and its combination of bit positions which has meaning.

Redundancy in Language

The transmission of information from one point to another always introduces some probability of making an error as long as the transmission is over a physical path. Binary information may be coded (by means of redundant bits) so that many of these errors may be detected or even corrected. The probability of a coded message being received at the termination of transmission with an undetected and/or uncorrected error can therefore be much lower than the original probability of having an error. The simplest of the codes is a so-called parity checking code which can detect single errors. In these codes the number of 1's in a given length sequence is counted and one extra bit (either 0 or 1) is added to the sequence so that the resulting sequence leaves an odd number of 1's (if odd parity is desired). Thus, should one error occur in any bit of the sequence, the parity check digit will point out the error, since it no longer makes the number of 1's odd. In addition, any odd number of errors can be detected by this method. Even parity is performed in the same manner except that the parity-checked word always has an even number of 1's. Other error detecting codes are available which will detect any given number of errors. Thus, by adding redundancy to a basic language, provision is made for detection or correction of errors.

*This set is referred to as binary coded decimal or BCD.

2. The Logical Algebra

The implementation of a digital data processor is based on the use of a logical language, Boolean algebra. From this it is possible to implement all logical statements based on the English connectives "and," "or," and "not."

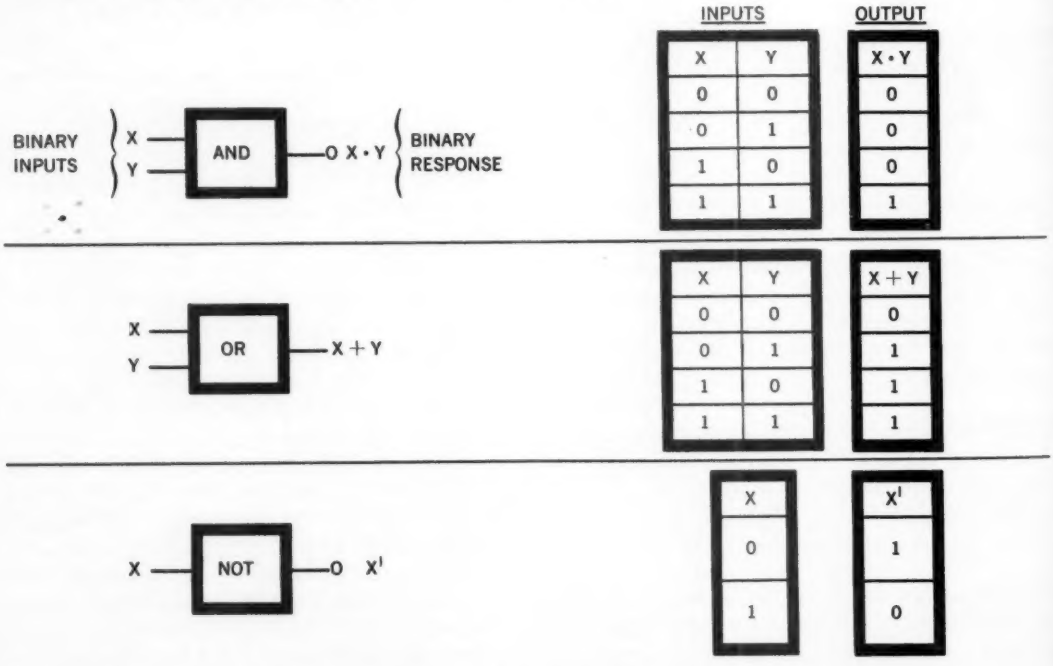


Figure 3. Truth table description of binary response to all possible input combinations

INPUTS		OUTPUT COMBINATIONS															
X	Y	0	X · Y	X · Y′	X	X′ · Y	Y	XY′+X′Y	X+Y	X′ Y′	XY+X′Y′	Y′	X+Y′	X′	X′+Y	X′+Y′	1
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

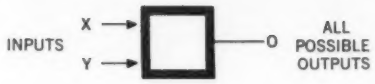
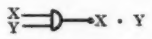
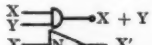


Figure 4. All the possible binary responses to two binary inputs

Boolean algebra as used by logic circuit designers is an algebraic description of these connectives. For two variables X and Y, the following chart gives the equivalent algebraic and circuit symbols.

Statement	*Algebraic Symbol*	*Circuit Symbol*
X and Y	X · Y	
X or Y	X + Y	
not X	X′	

From these three basic operations ("and," "or," and "not") a "functionally complete" set is formed. A "functionally complete" set consists of the basic operations which can be used to describe all the possible functions of n variables.*

Figure 3 shows the general situation, in which two inputs to a device result in a specific response to each input combination. Figure 4 shows all the possible responses to two inputs by a logical device with no memory. It is seen that all these functions can be described by "and," "or," and "not."

For example, since it is known that X + Y and X′ are a functionally complete set, therefore, any logical function of X and Y [e.g. (X + Y) + X′] can be implemented by circuits which perform the basic operations + and ′.

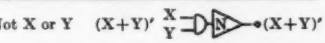
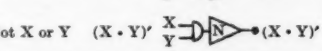
*The total number of possible functions of n variables is R^{R^n} where R is the radix and n indicates the number of variables. Therefore, in the binary case the radix is 2, so that $2^{2^2}=16$ gives the number of possible functions of 2 variables as described in Figure 4.

In Boolean algebra, the functionally complete sets which are usually of interest are:

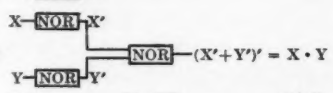
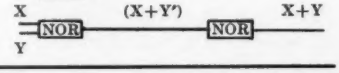
1. X + Y and X′
2. X · Y and X′

In many instances all three operations are used together since the increased versatility can often compensate for the logical redundancy.

Two other functionally complete sets are also of interest. They are:

	Statement	*Algebraic Symbol*	*Circuit Symbol*
1. The Pierce stroke: (NOR)	Not X or Y	(X+Y)′	
2. The Sheffer stroke: (NAND)	Not X or Y	(X · Y)′	

These are of particular value in that each of these by itself can implement all logical statements. For example, it is possible to build a logical system entirely with "NOR" operations, in which the "and," "or," and "not" connectives are made up entirely of NOR's, i.e.,

Statement	*Algebraic Symbol*	*Circuit Symbol*
Not X:	X′	
X and Y	X · Y = (X′+Y′)′	
X or Y:	X+Y	

The equivalency (x′ + y′)′ = xy is based upon a defined relationship in Boolean algebra, known as "DeMorgan's Theorem."

The Sequential Variable

Since data inputs into a data processing device usually occur in a sequential manner, the analytical tools must also be sequential. Thus, the use of combinatorial Boolean algebra as a description of data processor operations must extend into the time domain.

This requires that the processor must have memory, so that previous inputs or previous states of operation are known at the present time. The "state" of the machine is usually a recorded memory of what has happened prior to the present. To further define the situation:

If S(n) is the state of the machine during the nth time,
X(n) is the input during the nth time,
and Z(n) is the output during the nth time,
then the functional equations for sequential operations can be described as:

$$S(n+1) = F[S(n), X(n)]$$

and

$$Z(n+1) = G[S(n), X(n)]$$

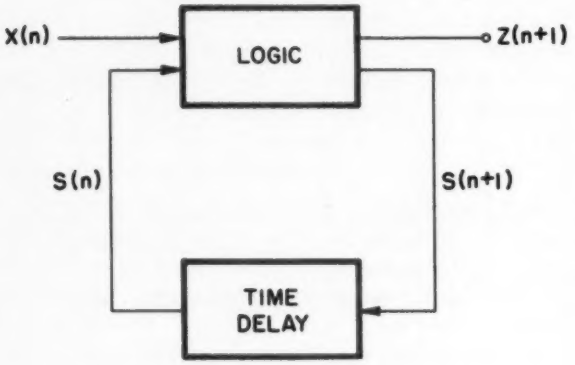


Figure 5. Model of sequential logic circuit

These equations explain that the next state of the processor depends upon the present state and present inputs to the processor; and that the next output depends upon the present state and present inputs. Thus, via the medium of "states," memory has been added. This is diagrammed in Figure 5.

Two types of sequential operations can be classified. One is asynchronous operation, in which each memory state lasts as long as the inputs remain. The other is synchronous operation, in which a clocking device is used to supply basic timing information.

The synchronous method is the more common one, in which all events are scheduled in a precise manner. For example, if either X or Y are binary inputs which operate a memory device (M) during the fifth timing pulse, the algebra is extended, so that:

$$M = (X + Y) \cdot t_5$$

This describes the logical statement: "M" will operate if X or Y occur, and the occurrence is coincident with timing pulse five. In this manner, no operation can occur unless it is allowed for in the logic scheduling.

Also, the machine now remembers this information for any future operations which depend upon M. If after t_5 the state of "M" indicates that it is in the operate condition, this is the means for the data processor to remember that X or Y actually did occur at time 5.

With the tools summarized above, a data processing system can be postulated on paper. The next step is the realization of these concepts with electronic circuits.

3. Building Blocks

The circuits which implement the logical algebraic operations described above are commonly referred to as building blocks. Each electrical block is used to facilitate the construction of the next larger electrical structure called a subsystem. The use of building blocks is not a new concept. The basic principle is as old as the Egyptian pyramids where pre-cut stones were placed together to form a larger structure. In more recent times, building block concepts have been used in many other areas such as prefabricated shipbuilding, and home construction. The primary consideration in determining the structure of a given digital building block is based upon the logical, storage or timing function it is to perform. The basic logical functions are the "and," "or," and "not" operations previously described.

The input and output characteristics of these devices are determined by means of a comprehensive analysis of system requirements. The requirements are essentially based upon loading, multiplicity of inputs, and reliability of each building block. A typical list of building blocks which have been developed by Raytheon is shown below in a functional arrangement.*

RAYTHEON BUILDING BLOCKS
(CADPO)

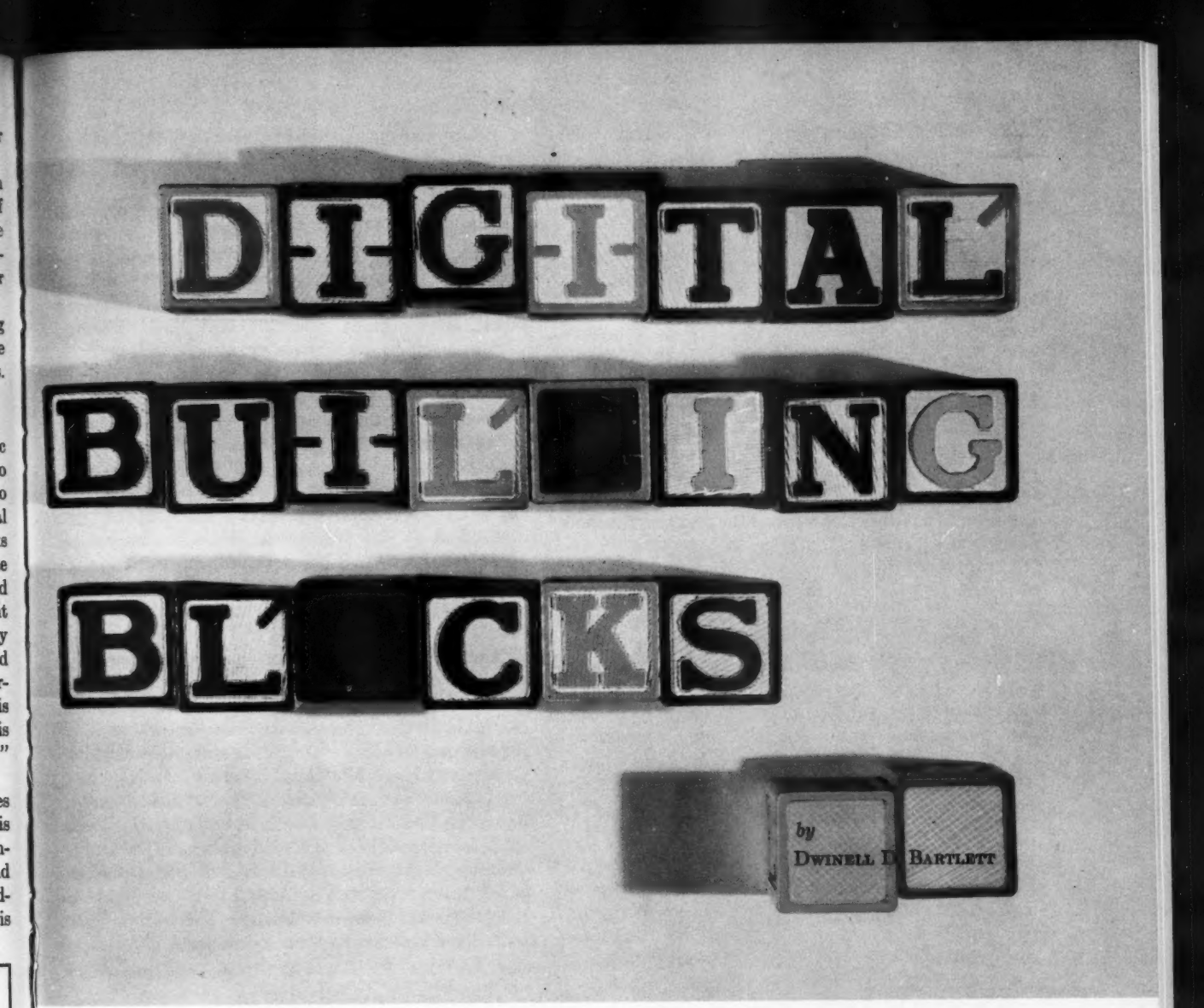
LOGIC FUNCTIONS (NO MEMORY)
AND gates
OR gates
Not (Inverter)
NOR (Not Or)
NAND (Not AND)

TIMING FUNCTIONS
One-Shot (Monostable Multivibrator)
Clock Oscillators

SIGNAL RESTORATION AND SPECIAL PURPOSE
Schmitt Circuits
Pulse Amplifiers
Gated Pulse Amplifiers

STORAGE FUNCTIONS
Flip-flop (Bistable Multivibrator)
Memory Planes
Magnetic Shift Registers

*Further discussion appears elsewhere in this issue in the article "Digital Building Blocks" by D. Bartlett.



IN LITTLE more than a decade, the data processing field has become an industrial giant. By the end of 1959, some 10 years after the first electronic computers were put into operation, 541 large-scale computers had been installed, with 200 more on order. At the same time, 645 medium-scale computers had been installed, an 88% increase over the previous year. Installations of small-scale computers totalled 2400, an increase of 76% over the previous year.[1]

Even more impressive is the expansion potential of the field. New applications constantly arise from spectacular new developments such as ultrafast switching devices, micro-miniaturization of circuitry, and semiconductor growth of complete circuits. Applications possible with presently available equipment are also expanding as the demand for data processing equipment increases. Perhaps the greatest changes in data processing in the past decade have come about through the development of solid state components such as transistors, diodes, etc. The present-day demand for data processing equipment is almost exclusively for higher speed, transistorized equipment. Although many different types of data processing equipment are being built, those using solid state circuitry have at least one thing in common: building block packaging. The building block concept is particularly applicable to the data processing field where logical switching techniques are used to handle data.

[1]John Diebold, "Experience, 1959, in Automatic Data Processing —A Review," Computers and Automation, Vol. 9, Nos. 7 and 7B, p. 10-12 (1960).

Switching techniques are quite well defined, and because of their nature, only a few different types of circuits will perform all the logical functions necessary for large-scale systems.

The functions which completely describe the internal operations of any size data processing equipment are *logic*, *timing*, and *memory*. *Logic* may be defined as the inter-connection of on-off circuit elements to perform a specific mathematical or logical function. A simple example of logic is a system of switches in two different locations for the same electric light. The light goes on if it was previously off and either switch position is changed. Similarly, it goes off if it was previously on and either switch position is changed. There is a logical decision with each change of switch position. Basic logical operations may be defined by truth tables showing the values of the variables and the resulting function values. (See Figure 1.) The circuit of Figure 2 gives the NOT-AND function in Figure 1, if only two of the seven inputs are used. *Timing* is considered to be the generation of system clock pulses or necessary logical delays. *Memory* is the storage of data; e.g., the electric light switches above have memory in that the light stays on as long as the switches remain in the positions that made the light go on. This is, of course, mechanical. The memory function in building blocks is electrical, but the effect is the same through electronic switching. Memory may be incorporated in both logical and timing functions.

Relatively few circuits are necessary to perform the above functions. These, together with a few special circuits for pulse shaping and buffering of data, plus special input-output circuits for particular problems in communication with equipment outside the data processing system are all the circuits necessary to completely define an entire system. This makes it possible to design circuits as building blocks for almost any data processing application.

An application of building blocks is shown in the computer block diagram of Figure 3.[2] The input could be punched cards, typewriter, paper tape, and magnetic tape, among others; the output, the same as the input possibly employing visual display; the auxiliary memory, magnetic tape or a magnetic drum, among others. The memory refers to high speed memory, usually magnetic cores or magnetostrictive delay lines. The arithmetic unit performs arithmetic operations. The control unit directs any desired operation of the whole or any part of the system.

The operation of this elementary computer can be explained quite simply by the analog of a person using a desk calculator. The calculator may be thought of as the memory and arithmetic units of the computer; i.e., it "remembers" the numbers added, subtracted, multiplied, or divided, and it does the arithmetic. The keys on the calculator would be analogous to the control unit, and the person thought of as the input and output units. Pencil and paper would be the auxiliary storage of intermediate results and also permanent storage of input and output information.

With the exception of the input and output units, and the auxiliary memory unit, the entire system of Figure 3 can be implemented using the standard building blocks. Standard building blocks are a logically consistent set of circuits capable of being joined together to produce all the required functions of a digital system.

This example may be extended in that the data being evaluated on the desk calculator first had to be acquired, interpreted, and put into a form acceptable to the calculator. These operations can also be done electronically using standard building blocks. Thus, there

[2]D.D. McCraken, *Digital Computer Programming*, John Wiley and Sons, Inc., New York, N.Y., 1957.

INPUTS		OUTPUT
A	B	$(A \cdot B)'$
0	0	1
0	1	1
1	0	1
1	1	0

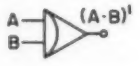


Figure 1. Truth table for the logical statement "NOT A AND B"

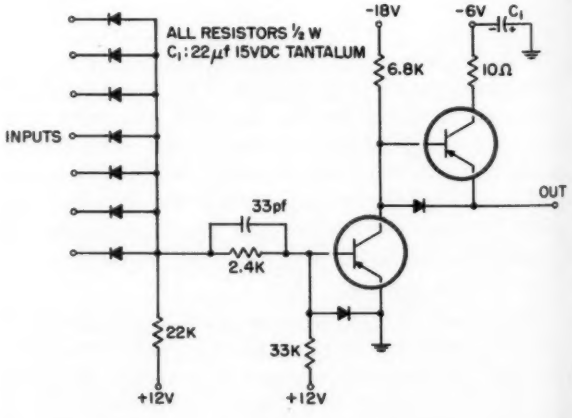


Figure 2. Circuit producing the NOT-AND function of logic

are four major areas[3] of application for the building blocks:

1. Data Acquisition which consists of gathering and translating information to digital form, such as A/D converters;
2. Data Evaluation which includes mathematical operations done on the data such as the arithmetic unit of the computer;
3. Data Handling which includes data selection, sorting, mixing, correcting, monitoring, format translation, searching, and reading;
4. Data Display which is simply the communication between the machine and the human operator.

Thus only the few circuit types making up the standard building blocks are required to construct equipment to perform most of the necessary operations in a complete cycle of data flow.

The standard building blocks should also be completely defined as a load to other blocks and as to what the block itself is capable of driving. A computer using this information, together with the function of the block, could implement system functions. For example, if the loading characteristics and functions of all building blocks were stored in the memory of a computer, the system functions to be implemented could be fed to the computer, which would then display a solution to the implementation problem, together with all wiring connections. This would eliminate errors in implementation. However, since design and packaging is done for general application, great care would have to be exercised to obtain the optimum in reliability, versatility, and economy.

Advantages of building blocks, other than those inherent in the computer example, include: a) new circuit designs are not necessary each time a new system is

[3]Clark F. Crocker, "Digital Data Processing," Internal Report, Raytheon Co. (February, 1959).

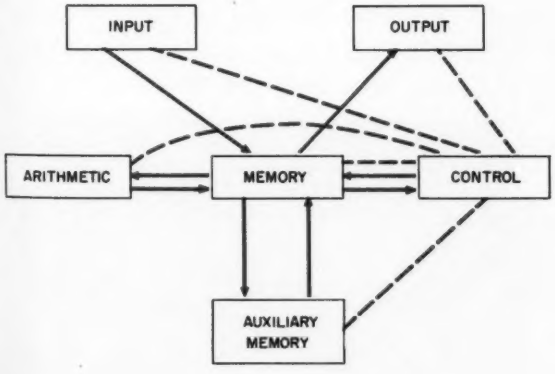
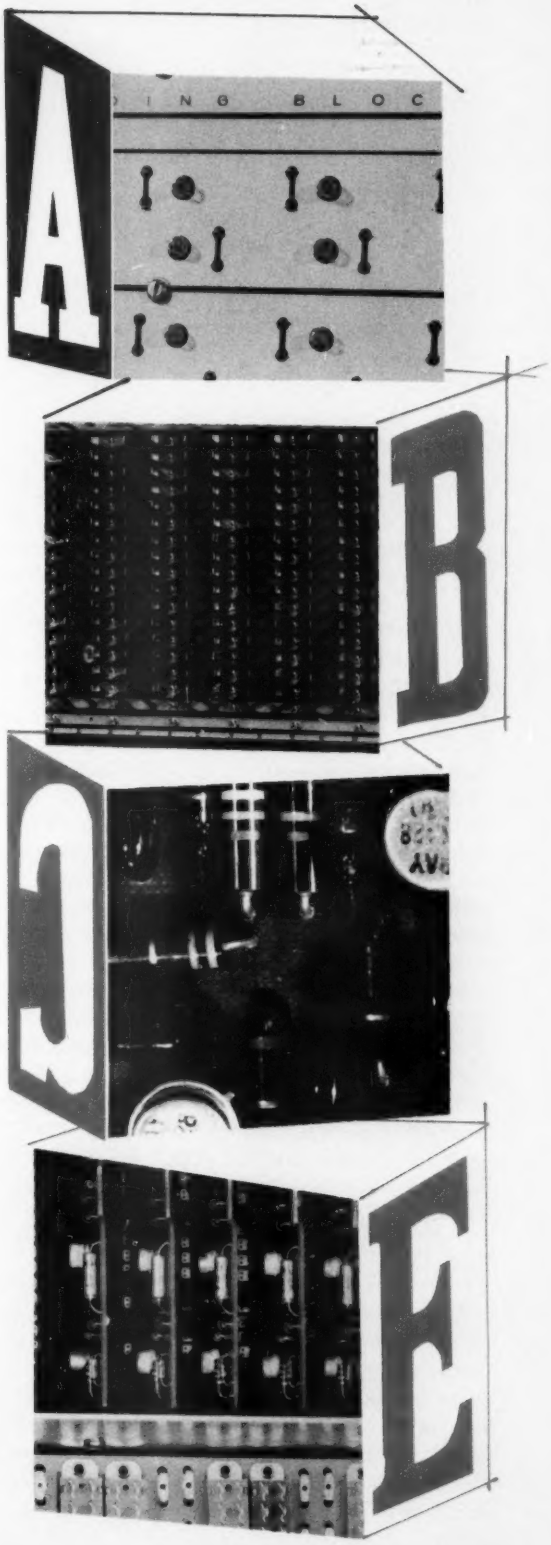


Figure 3. Functional parts of a digital computer and their relationships

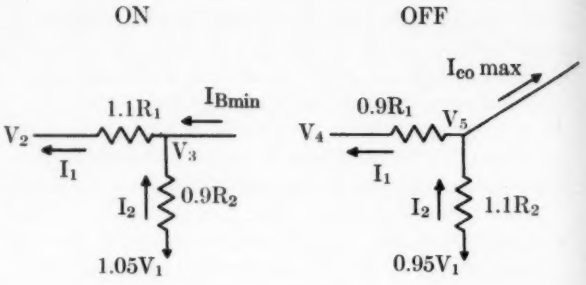


proposed because they are pre-designed with a complete set of rules for their use; b) service and maintenance problems are reduced for equipment in the field; c) only a relatively small inventory of spare parts is necessary; d) more economy is realized in mass production because of the small number of different type assemblies; and e) more accurate cost estimates are possible, an especially important consideration for commercial equipment applications.

There are quite a number of building block lines offered by different companies today. Anyone wishing to build a system using purchased blocks might become rather confused as to which ones to buy because of wide variations in price, circuit sophistication, versatility, and type of packaging. Probably the most important characteristic to be considered is reliability, because "down time" in data processing equipment (a computer, for example) proves to be expensive.

The reliability of a circuit is determined, to a great extent, by the *combined* reliability of the components used in the circuit; i.e., the more components used, the less reliable the over-all circuit becomes. Therefore, the foremost consideration in attaining high reliability is to use only highly reliable components. However, the reliability of the components can be assured only by proper circuit design: thus, the design should be such that all components are a safe margin away from their maximum ratings. In a properly designed circuit, the reliability of the finished assembly should be little less than the limit imposed by the combined components. This can be accomplished by considering worst-case conditions in circuit design. In the author's opinion many of the building blocks for commercial application on the market today will not pass a worst-case analysis. These worst-case conditions are the criteria used by Raytheon engineers in the design of their building blocks for commercial equipment.

One example of these conditions is the following: Suppose one is to design the bias network for the circuit of Figure 2. Two conditions must be considered—when the transistor is ON and also when it is OFF. For the circuit to be reliable, operation must be assumed under the worst possible operating conditions. In the ON case, these conditions would be: a) that one has a transistor with minimum beta, b) the ± 5% resistors are off in their worst directions by their tolerance, and c) that the power supplies are also off by their maximum amount. This, however, is still not enough because this worst-case may occur at or near end-of-life of the transistors, diodes, and resistors. Therefore, only ¾ minimum beta can be used to allow for decrease in beta with age, and resistors must be allowed ± 10% variation for change in value with age. The argument is similar for the OFF case. Therefore, the design of the bias network would be as shown using a PNP transistor with 0 and —6 volt levels.



$I_1 - I_2 = I_{Bmin}$ (1)

$I_1 - I_2 = -I_{co}$ (2)

where, $I_{Bmin} = I_c/(¾\ B_{min})$; $V_2 = -6 \pm$ diode and/or transistor drops; V_3 includes maximum drop across transistor junction; 1.1 R_1 and 0.9R_2 allow for 10% variation for worst case; 1.05V_1 = 5% variation in supply; I_{co} is determined for desired temperature range; V_4 = 0 ± diode and/or transistor drops; V_5 = back bias voltage for transistor.

Solving the two equations simultaneously gives values for R_1 and R_2 such that sufficient base current will flow under worst conditions, and in addition, that the transistor will certainly be off at the highest specified temperature—also under the worst operating conditions. Designing circuits in this manner, and also exercising care that components are operating well away from their maximum ratings, assures maximum dependability.

Once designed, the circuits must be packaged so that a versatile economic building block is obtained. In many applications, building blocks must be very compact to comply with equipment size requirements. Considerable effort is now being exerted in the design and development of microminiaturized building blocks or modules. Raytheon is one of the companies doing work in this field. These microminiature blocks are, at the present time, more expensive than the other blocks mentioned. For applications where small size limitations are not required the conventional building blocks are best suited to do the job.

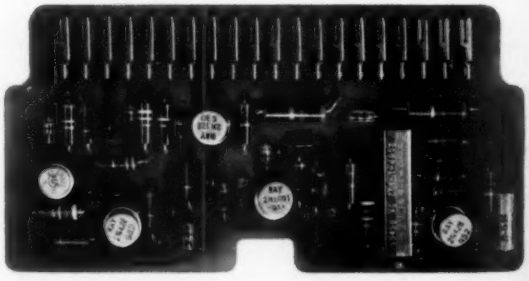


Figure 4. A typical digital building block

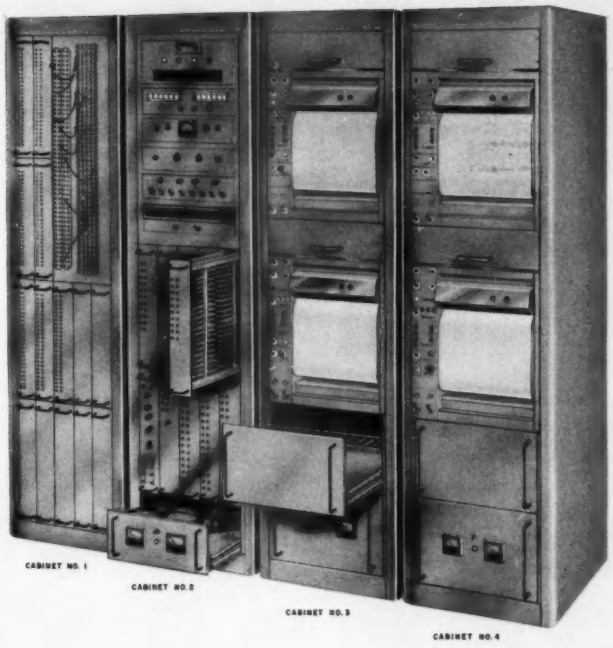


Figure 5. Artist's conception of equipment proposed for a PCM telemetry data-reduction system. An added feature of these panels is the ease of access to the circuitry since the panel may be pulled out and tipped 90 degrees.

Raytheon Building Blocks

Raytheon's Communications and Data Processing Operations presently has a complete line of 1Mc building blocks, in addition to a nearly complete line of 5 and 10Mc blocks for application in digital data processing. These blocks are to be used primarily in commercial equipment but with very little modification will meet military specifications. The blocks are packaged on a 2½ x 5-inch card with connectors so that they may be removed and replaced at will, as shown in Figure 4. Forty of these cards make up one 3½ inch panel for a standard 19 inch rack which may be mounted horizontally or vertically. As an example Figure 5 is an artist's conception of equipment proposed for a PCM telemetry data-reduction system. An added feature of these panels is the ease of access to the circuitry since the panel may be pulled out and tipped 90 degrees.

Although the building blocks mentioned above are functionally complete in that they provide all the functions necessary for a data processing system, these would not be practical for storage of large amounts of data or for low speed applications. For these reasons considerable work has also been done on magnetic building blocks. Magnetic cores are highly reliable and quite inexpensive—thus their value for large volume storage and low speed data processing applications. The disadvantage of cores is their relatively slow speed of operation compared to transistorized building blocks. However, core storage is referred to as high speed storage in a computer because here the comparison is with other types of storage such as magnetic tape, magnetic drums, etc. Raytheon presently has a magnetic line that operates at 100 kc, and a 500 kc line is the development stage.

Even though economical data processing systems with high volume storage can be completely defined using the building blocks described, there is always a search for even more economy, versatility, and reliability. One such project now in progress at Raytheon is a study of the feasibility of stacked NOR elements. The NOR element is a multi-input, multi-output, single-stage transistor inverter. The logical operations of this one element are such that a complete system may be implemented using this single simple circuit. Its advantages lie in the fact that greater reliability is attained because of simplicity, and production costs are less because only one type of building block is involved. The main disadvantage is that performance of some functions is awkward with only one type of circuit and the amount of circuitry necessary for some systems is usually greater than it would be if other building blocks were used. This does not mean, however, that the system would be automatically more expensive. The purpose of the feasibility study of the stacked NOR project is to investigate the possibility of significantly decreasing the amount of equipment necessary to solve problems containing many variables.

The building blocks designed by Raytheon have been used in equipment such as high speed A/D converters, a tropospheric scatter communication system, pseudo-random noise generators, data converters, and a small limited general purpose computer which was designed to check the operation of the building blocks. These blocks have proved to be what they were designed to be; namely, economical, versatile, and reliable.

ANALOG TO DIGITAL CONVERTER TECHNIQUES

by CLARK F. CROCKER

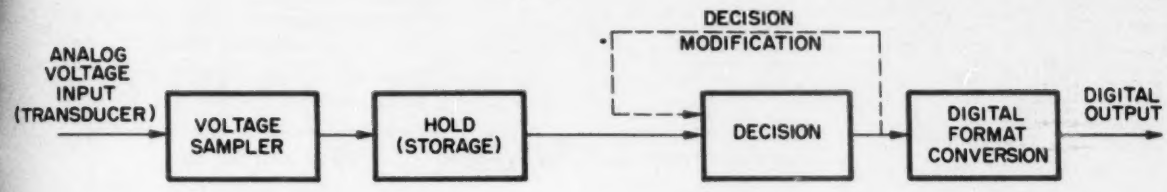


Figure 1. Generalized A/D converter

THE PROBLEM of translating an analog voltage into a digital signal has become more important with the advancement of digital techniques and digital computer applications. The device normally used for converting an analog voltage into binary coded signals is appropriately called an analog to digital (A/D) converter. In this paper the basic operation of A/D converters will be discussed and some specific types examined.

Figure 1 illustrates the generalized signal flow which is usually required to perform an A/D conversion. The information signal from most transducers is of a continuous nature. The amplitude of the continuous signal is analogous to the physical quantity being sensed, hence the common usage of the word analog. This continuous signal can be represented by means of a discrete or discontinuous signal with very little loss of information, provided that discontinuities occur often enough to produce a step-like representation of the continuous signal. The discrete signal is obtained by sampling a continuous signal periodically. This sampling operation is quite similar to the observation of a continuous waveshape through a shutter mechanism such as a camera. The aperture of an A/D converter is the time necessary for the converter to look at the input analog signal in order to obtain sufficient information to encode its instantaneous amplitude. This sampling process is illustrated in Figure 2. The pulse resulting from this sampling operation is commonly referred to as a pulse amplitude modulated (PAM) signal since its amplitude is proportional to the peak amplitude of the continuous signal at the instant at which it was sampled.

In some converter units the peak amplitude of the PAM signal is stored (or held) until the next sample is taken. This is done, however, only if the converter is incapable of making all of its necessary decisions within the time occupied by the sampled PAM signal. It should be noted that not all A/D converters have sample-and-hold circuits. In these cases the PAM signal must be supplied directly to the decision portion of the converter from external equipment.

The function of the decision portion of an A/D converter is to compare the peak amplitude of the PAM signal with an internally generated reference voltage. In some converters a decision is made only when the input signal is equal to or greater than the internally generated reference signal. In other converters several decisions are made during each sample interval and the reference signal modified on the basis of each decision. The details of these decision processes are discussed below in relation to specific converter types.

The last step in A/D conversion is format conversion, which is a permutation process. For example, a serial binary representation may be modified into a parallel binary representation. The process may also be reversed to perform parallel to serial presentation. Another example is the conversion of a unit distance binary code (Gray Code) into an 8421 binary code. It should be noted that a format converter is not always necessary. Quite often the coded output from the decision unit is adequate for presenting signals to the next unit in a digital system.

The operation of A/D converters can best be illustrated by examining some of the particular types and the techniques involved in their operation.

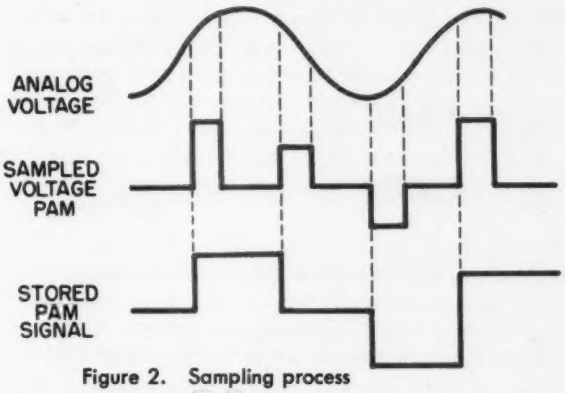


Figure 2. Sampling process

The Ramp A/D Converter

The operation of a ramp converter (Figure 3) is initiated by means of a sample gate pulse which is applied to the input of a ramp generator. The ramp generator produces the triangular waveshape shown in Figure 4, waveform A. As this rising voltage becomes equal to or greater than the zero reference signal applied to comparator No. 1, a pulse is produced which is used to set a control flip-flop. When the rising voltage becomes equal to or greater than the analog voltage ap-

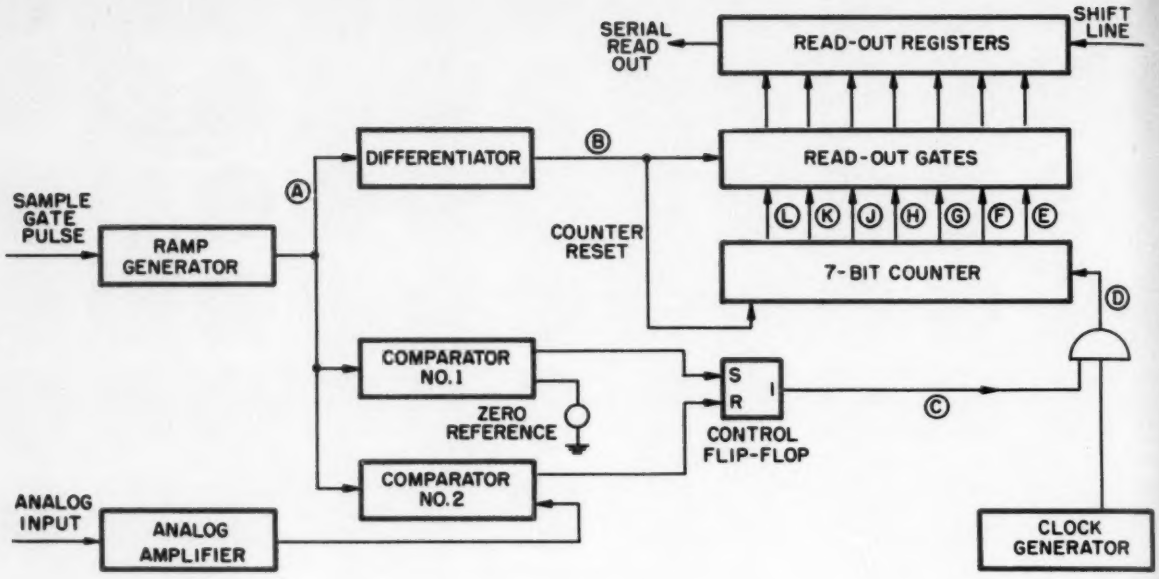


Figure 3. Ramp A/D converter

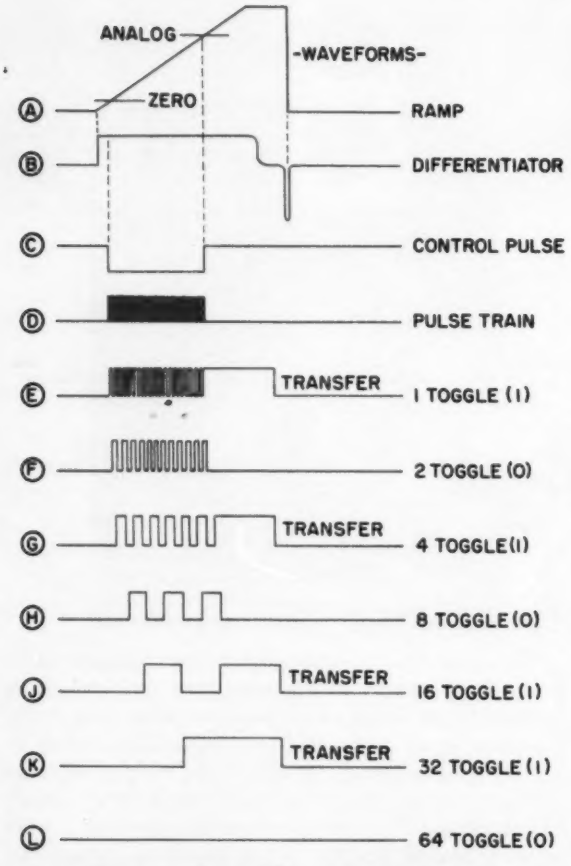


Figure 4. Ramp A/D converter waveforms

plied to comparator No. 2, a pulse is produced to reset the control flip-flop. The result of this operation is to produce a control pulse, the duration of which is proportional to the amplitude of the input analog signal. This control pulse is then used to gate clock pulses (which are a periodic train of timing pulses) into a counter which starts at a count of zero. The number of pulses allowed to enter the counter is proportional to the pulse width of the control pulse. Therefore, the final content of the counter is proportional to the amplitude of the analog signal. After the ramp voltage reaches a maximum it is returned to its initial value. The trailing edge of the ramp voltage is used to generate a reset pulse which reads out the contents of the counter into an output register and resets the counter to zero.

The contents of the output register are then read out sequentially, that is, one bit at a time, as each shift pulse is applied to the output register. It is also possible to read out the contents of the counter in a parallel manner on the lines between the read-out gate and the output register.

One of the most serious problems associated with this converter is that it is essential that the amplitude of the PAM sampled pulse remain relatively constant during the aperture time. In this converter the aperture is equal to the duration of the control pulse. The expression "relatively constant" means that the amplitude of the analog signal will not vary enough to produce a change of more than one count in the counter.

It is necessary to hold the input analog signal relatively constant in order to achieve reasonable converter accuracies and eliminate ambiguities in the

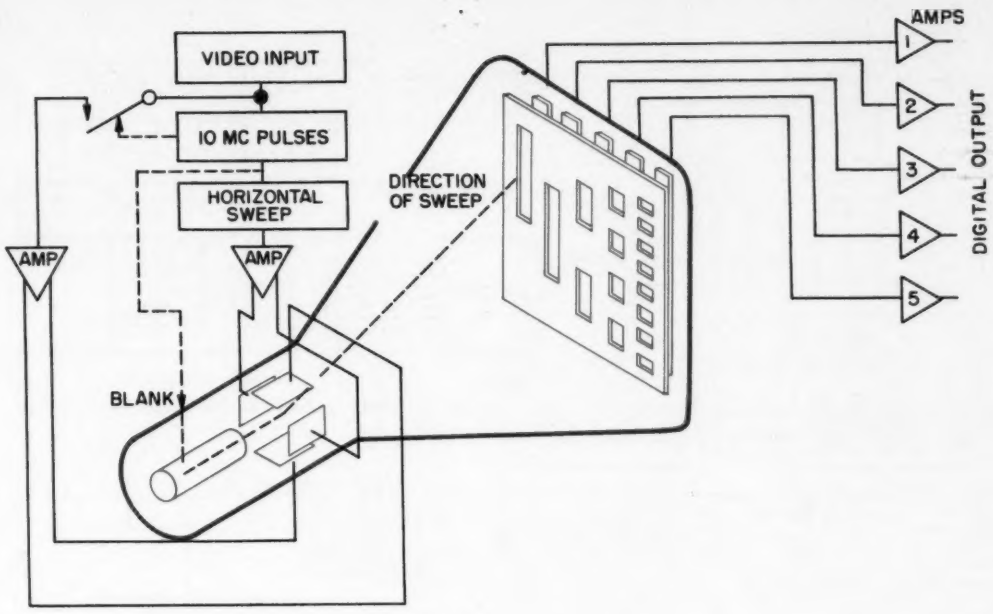


Figure 5. Cathode ray oscilloscope A/D converter

digital output. For example, if 100 microseconds is required to encode a maximum amplitude analog signal to an accuracy of 1%,* then it is essential that the input voltage not vary by more than 32 cps. At any frequency above 32 cps the signal will change by more than one count during the sampling interval, yet the converter is capable of sampling at 10,000 samples per second and sampling theory indicates that frequencies approaching 5000 cps can be encoded. This upper sampling limit can be realized by utilizing a sample-and-hold circuit which samples the analog signal during a very short time interval and maintains the peak amplitude of the PAM signal for a long interval. It should be noted that the sampling interval must be short enough so that the amplitude of the analog signal, when varying at the highest acceptable frequency, will not change by more than the equivalent of one count during this sampling interval. Furthermore, the amplitude of the PAM pulse must be held accurately for the full aperture time.

Ramp encoders have been built to accuracies exceeding 0.1% at sampling rates greater than 1000 samples per second. Raytheon has developed units which exceed these specifications and have a unit power requirement of less than 0.25 watt.

Cathode Ray Tube A/D Converter

Figure 5 depicts a cathode ray oscilloscope A/D converter designed to achieve a sampling rate of 10 million samples per second. The video input is sampled and held so that there is no vertical component of motion while the horizontal sweep circuit directs a narrow electron beam across the face of the code plate. The sampled video input is directed to the plates which position the beam vertically. As the beam moves it impinges on the electrodes behind the code plate if there is an opening. The code plate is so designed that consecutive Gray codes† appear across its surface. The 10 Mc sampling pulse blanks the electron beam so that the output amplifiers do not produce an output during the return of the sweep. Devices of this type have been built with accuracies of approximately 1% (7 bits). Parallel readout, if desired, can be obtained by retiming the outputs or by forming a horizontal fan-shaped beam within the tube.

This device is similar in method to shaft position encoders or code wheels where alternate surfaces of conducting and non-conducting material are arranged concentrically and sampled with brushes. Another type employs concentric rings of transparent and opaque surfaces which pass or block light rays from impinging on photoelectric sensors, thus producing the required code. Some of these devices suffer from ambiguities which occur when the device is oriented between codes; special codes are often used to circumvent this problem.

Although the cathode ray tube encoder achieves high sampling rates with commensurate accuracies, it suffers the disadvantage of decreased reliability, increased power requirements and size and the necessity for high voltage supplies. Note also that although this device requires no reference voltage, the output of the video

*The accuracy attainable with an A/D converter is a function of the number of increments into which the maximum amplitude of the input signal can be divided. In a seven-bit converter the number of increments is 2^7 or 128.

†See Appendix

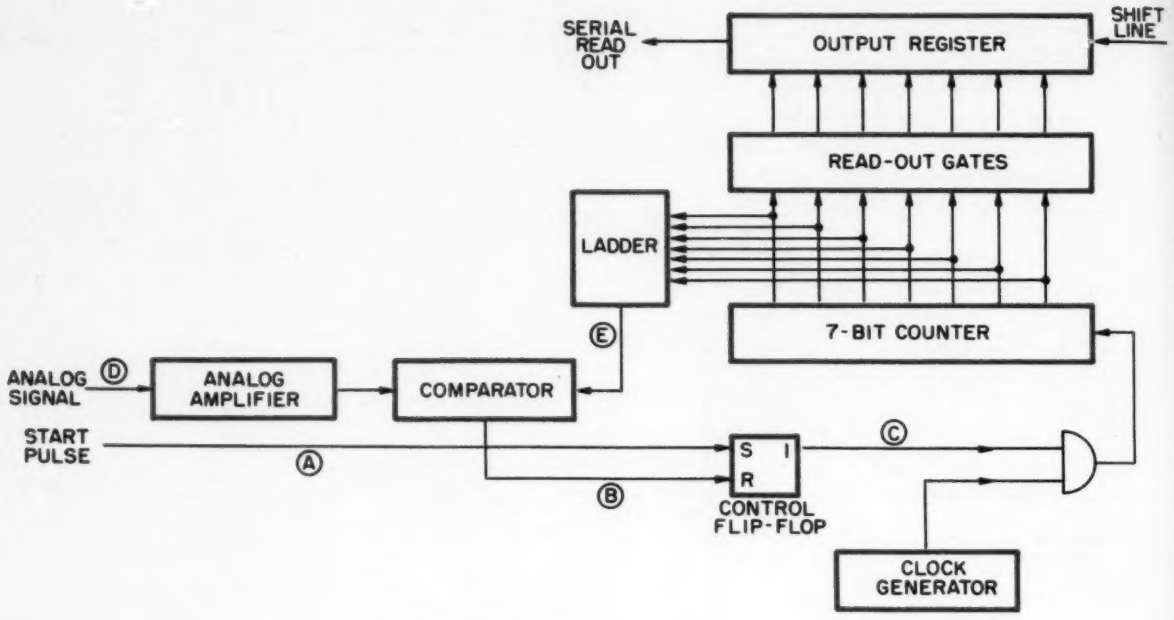


Figure 6. Staircase converter

amplifier must provide the required accuracy and stability. The high voltages required by the cathode ray tube also must be stabilized to assure accurate deflection. For these reasons, other means have been sought to achieve high sampling rates at increased accuracies.

Feedback Converters

Thus far we have been concerned with A/D converters which have been characterized by the absence of feedback. We shall now consider three converters which are feedback encoders; they obtain the feedback and consequently the conversion to digital code by digital-to-analog conversion.

Staircase Converter

The operation of the staircase converter shown in Figure 6 is similar to the ramp converter except that the ramplike voltage is discrete rather than continuous.

Initially a start pulse is used to set a control flip-flop. The control pulse from the flip-flop is used to gate a series of clock pulses into a counter which has an initial value of zero. The accumulated contents of the counter are decoded by means of a resistive summing network called a ladder. This ladder network is designed so that an output voltage called a staircase (see Figure 7) increases discretely as the number of input pulses to the counter increases. Thus, this ladder network is a digital-to-analog converter, the output of which, in this application, is a staircase voltage. This voltage continues to increase until it exceeds the amplitude of the analog signal by less than one count. At this time the comparator generates a stop pulse. The stop pulse resets the control flip-flop, thus terminating the flow of clock pulses into the counter. The content of the counter is now proportional to the amplitude of the input analog signal. The stop pulse is further used to transfer the contents of the counter into the output register and to reset the counter to zero.

The staircase converter, like the ramp, must use a sample-and-hold device when the input analog signal is of a high frequency nature. In the staircase converter, however, the ramp voltage can be implemented more easily.

Staircase generators are used as peak detecting devices. By making at least one comparison per unit change in the analog input they effectively track the input signal. Since the device does not count down, it can be implemented so that it will remain at the digital value corresponding to the peak of the analog voltage after the analog signal decreases. For example, this approach has been used to convert peak output signals from a mass spectrometer scan to numbers punched on IBM cards for direct analysis by a computer.

By use of a forward-backward counter the staircase encoder can continuously track a single channel input, thus making available a continuous digital readout at the discretion of an external interrogating device.

Logical Approximation Converter

A method of A/D conversion which is faster than that used in the staircase converter involves the buildup of a feedback reference voltage. This is performed in a trial-

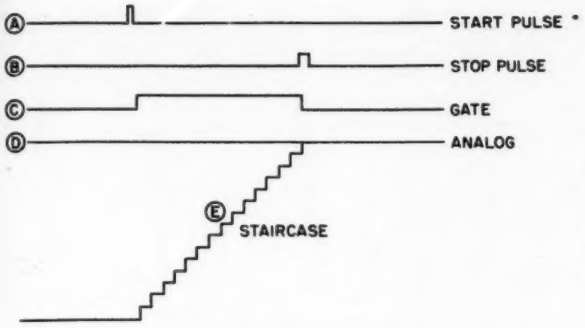


Figure 7. Staircase converter waveforms

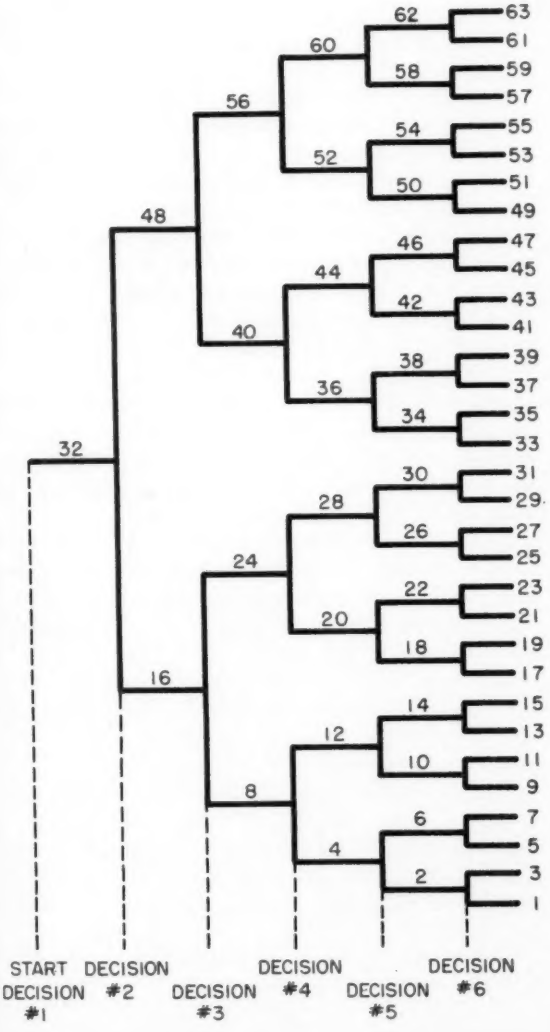


Figure 8. Tree diagram

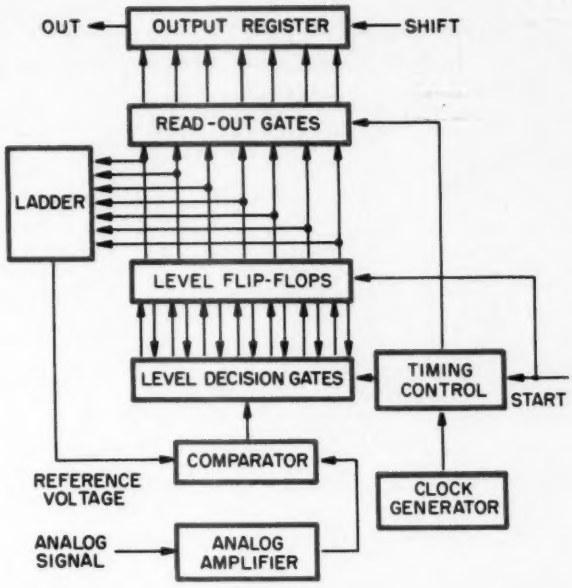


Figure 9. Logical approximation converter

and-error fashion known as logical approximation. In the first approximation, a feedback voltage equal to half the maximum value of the input analog signal is tried. If it is too large, it is discarded and a one-quarter scale voltage is tried. If the half scale voltage is too small, a one-quarter scale voltage is added to the first approximation. The result is a three-quarter scale reference voltage. This process is continued until all bits to the least significant have been encoded. The conversion process is then complete. The decision-making processing is exemplified in Figure 8. Note that for seven bits, only seven tries are necessary whereas the staircase device would require 127 tries. In the logical approximation method the number of tries is equal to $\log_2 127$ or 7. It is therefore a much faster coding method for devices having comparable speed limitations.

A block diagram of a logical approximation converter is shown in Figure 9. The operation of this encoder is as follows. A start pulse is simultaneously applied to both the timing control and the level flip-flops. The level flip-flops are set in such a manner that their states will cause the output of the ladder network to be at a value of voltage which is equal to one half the maximum permissible value of the analog input signal. The comparator then makes a decision as to whether the input analog signal is greater or less than the reference voltage from the ladder network.

The state of the level flip-flops will be modified in different ways depending on whether the analog signal is greater or less than the reference signal; if greater, the flip-flops will be altered in one manner; if less,

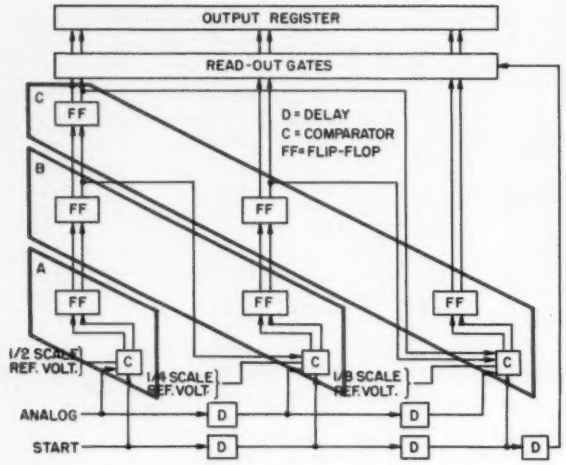


Figure 10. Feed-forward A/D converter

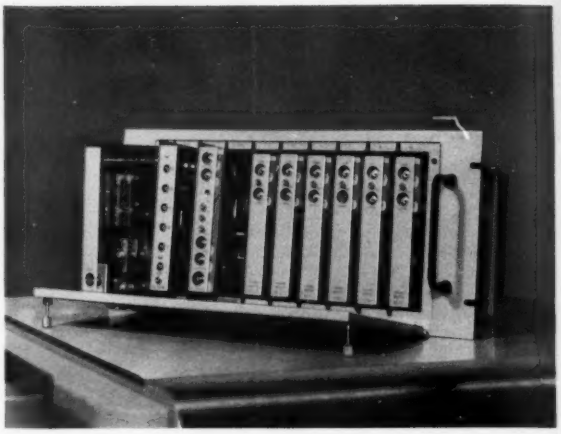


Figure 11. High speed feed-forward A/D converter

in another. The end result of either of these modifications is that the output of the ladder network will change so that the input analog signal will be ready for comparison with a new reference signal. This decision-making process is the logical approximation procedure and is the same as previously described. At the end of the last decision the states of the level flip-flops will reflect the amplitude of the input analog signal and consequently can be read into an output register for serial presentation or to be read out in parallel.

The sampling problems which are inherent to all of the previous converters apply to this one as well. The holding requirements for the PAM pulse are less stringent, however, because the aperture time is so much smaller.

A converter using this scheme is now being designed by Raytheon. Its accuracy is 10 binary digits or 0.1% and it operates at a speed of 0.1 microsecond per decision. Since it must make 10 decisions per sample, its maximum sampling rate is 1.0 microsecond per sample or one million samples per second.

Parallel-Feed-Forward A/D Converter

Raytheon has recently developed a technique of parallel-feed-forward encoding of analog signals. With this technique it is possible to design a converter with an aperture theoretically equal to zero, but in practice equal to 10 to 20 millimicroseconds, and sampling rates up to and beyond 10,000,000 samples per second. In actual models utilizing this technique the sampling time has been reduced to the time to encode one bit and the aperture to a small fraction of the bit time. The result is the fastest converter presently available capable of six- to eight-bit accuracies.

In the conversion process, an individual comparator is used for each bit. Both the analog signal and the comparator outputs are stored so that each succeeding bit comparator has forwarded to it the results of all preceding comparisons.

This converter is composed of a number of logical approximation converters equivalent to the number of bits to be encoded. Each succeeding converter is capable of encoding one more bit than the preceding converter and utilizes the outputs of the previous converters in this encoding process. As seen in Figure 10, converter A is used to encode the most significant bit. The result of this encoding is fed forward to converter B which then utilizes it in encoding the second most significant bit. The results of both encoding operations are then fed forward to converter C for the encoding of the third most significant bit. This technique may be extended to as many bits as are desired. The speed of the converter is attained because converter A may be used to encode the most significant bit of a second sample while converter B is encoding the second most significant bit of the first sample. Thus, although the total conversion time for a single sample through this converter is equal to that for an ordinary logical approximation converter, the rate at which conversions may be made is inversely proportional to the time necessary to encode one bit.

This means that in an eight-bit machine, if the time necessary to encode one bit is 0.1 microsecond, the sampling rate will be 10,000,000 samples per second. The output of the converter may occur in either a parallel or sequential binary code at a bit rate of 80,000,000 bits per second.

Figure 11 is a picture of a high speed feed-forward A/D converter and its power supply.

Summary

Table I presents a summary of currently available

TABLE I

GENERAL CATEGORIES OF VOLTAGE TO DIGITAL CONVERTERS AND THEIR APPLICATIONS

LOW SAMPLING RATE HIGH ACCURACIES	MEDIUM SAMPLING RATE MEDIUM ACCURACIES	HIGH SAMPLING RATE RESTRICTED ACCURACIES
Logical Approximation Converters Ramp Converters Staircase Converters	Logical Approximation Converters Ramp Converters Staircase Converters	Cathode Ray Tube Converters Feed-Forward Converters
1 to 100 samples/sec. 0.005% to 0.01% accuracy above 1 megohm input impedance	100 to 50,000 samples/sec. 0.01% to 0.1% accuracy 10 kohm to 100 kohm input impedance	10^6 to 10^7 samples/sec. 0.1% to 2.0% accuracy below 10 kohm input impedance
Uses: Laboratory-dc measurements Logging systems Process control	Uses: Laboratory-quasistatic measurements Process control Instrumentation systems	Uses: Laboratory-dynamic and transient measurements Instrumentation systems (vibration measurements) Radar systems Communications systems (multiplexed audio or video) Spectroscopy

A/D converters and their general areas of application. Of course, it is desirable in a measuring instrument to keep accuracies, speed and impedances high. In general it becomes more difficult to maintain higher accuracies and impedances as the requirement for sampling rates increases. Fortunately most requirements demand less accuracy and input impedance as the bandwidth of the signal to be measured is increased.

APPENDIX

Unambiguous Codes

The problem of ambiguity in encoders such as shaft position devices and the cathode ray tube device can be illustrated by the following example.

The binary codes for the two consecutive numbers 15 and 16 are:

0 1 1 1 1
1 0 0 0 0

If the cathode ray encoder suffered a slight deviation from horizontal as it swept across a binary code plate, it would be possible to read out 1 1 1 1 1 which is the binary equivalent for 31 or 0 0 0 0 0 which is equal to zero. What is required is a code which permits only one digit to change from any number to the next so that either of the two numbers in question is read but no other. Such codes are known as nonambiguous or unit distance codes. Other names are cyclical or reflected binary. One of the most common of such codes is the Gray code. The code is characterized by the fact that the absolute value of a "1" in digit column J is given by

$$\sum_{i=0}^{i=J} 2^i$$

and the sign associated with it is positive for all odd numbered ones starting from the left and negative for all even numbered ones. As an example:

$$1010 = \sum_{i=0}^{3} 2^i - \sum_{i=0}^{1} 2^i =$$

$$2^3 + 2^2 + 2^1 + 2^0 - (2^1 + 2^0) = 2^3 + 2^2$$
$$= 8 + 4 = 12$$

The Gray equivalent of 15 and 16 is 0 1 0 0 0 and 1 1 0 0 0 respectively. It can now be seen that since the codes are identical with the exception of the most significant bit then the holes representing the codes 15 and 16 are unchanged with the exception of the first digit and no ambiguity in the digital readout is possible between the adjacent numbers.

Computation is seldom if ever done in Gray code. Usually Gray is translated into binary and the computation performed in the latter code. Because in Gray code each "1" stands for a summation of powers of two and the sign of successive "1's" alternates, a simple rule exists for translating from Gray code to conventional binary code. The rule is this: The most significant "1" remains unchanged. Each successive digit becomes complemented (a "1" made into a "0" and a "0" into a "1") as many times as there are "1's" preceding it in the Gray code number.

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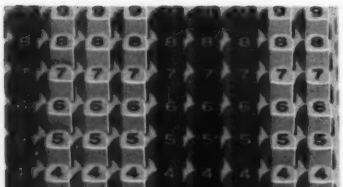
CENTRALIZED DATA PROCESSING



by EDWARD L. GILFIX

Introduction

WITH THE advent of solid-state, second-generation, data processing equipment, a new area of potential applications has arisen. This area is organized around the field of centralized data processing and draws upon the considerable experience that has evolved, of necessity, from military requirements. It reflects anew the next step forward in what appears to be a second industrial revolution.

Centralized data processing has, as a basic design characteristic, the integration of data inputs supplied from various remote generating sources. Thus, one centralized location serves many inputs rather than having separate processing at each remote location. A further descriptive characteristic is that centralized data processing, dependent upon the type of systems under consideration and their functional requirements, is often enhanced by ensuring that data input and output to the central processor is achieved on a real-time basis. That is, input data of an inquiry or quantitative nature serves to establish a sequence of processing operations and an appropriate system response, with essentially no time delay. The response is transmitted when required to the input source or other dependent peripheral elements in accordance with the type of inquiry or numerical content of the original information. This is done at speeds which result in a systems data flow being effectively continuous for the application under consideration.

A real-time, centralized data processing system basically consists of three major elements (Figure 1). They are: the remote *input device;* the appropriate *communica-*

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...A SYSTEMS PERSPECTIVE

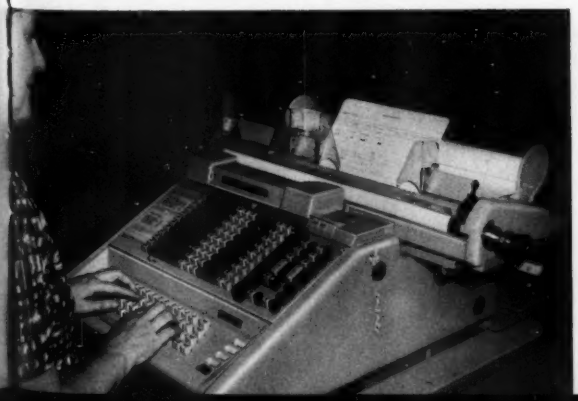
tion channel, i.e., microwave, telephone, coaxial cable; and the *data processing unit*. The integration of these basic elements with a rigorous systems design can result in a sophisticated data processing system with an inherent flexibility adequate to meet the requirements of a large number of potential industrial, commercial, and military users.

System Application

A real-time system, which also includes a general purpose computer, provides the user with a flexible system adequate to accommodate the data processing requirements associated with a variety of applications, such as:

COMMERCIAL and INDUSTRIAL

- Banking operations
- Inventory control
- Accounts payable
- Handling of reservations
- Machine and manpower scheduling



MILITARY AND SCIENTIFIC

- Remote recording of scientific experiments
- Radar input and evaluation
- Satellite tracking and control
- Missile detection and interception
- Prelaunch missile checkout and evaluation

In lieu of generally describing each of the above applications we will consider in detail a specific area which illustrates the systems requirements associated with the new family of second-generation, real-time, integrated data processing systems. Specifically, we will discuss the banking field in terms of savings bank requirements and concentrate on the application of integrated data processing to the jobs of deposit accounting and mortgage-loan accounting.

Centralized Accounting Operations and Savings Bank Objectives

Preliminary to the design of a system, whether integrated or decentralized, it is requisite that the objectives of the new system be consistent with those of the one it is replacing. With this in mind, the following is a summary of the basic parameters in the design of a centralized system for the use of a group of savings banks:

1. Each participant bank in the system is treated as an autonomous unit.
2. The system provides a "go no-go" response to each

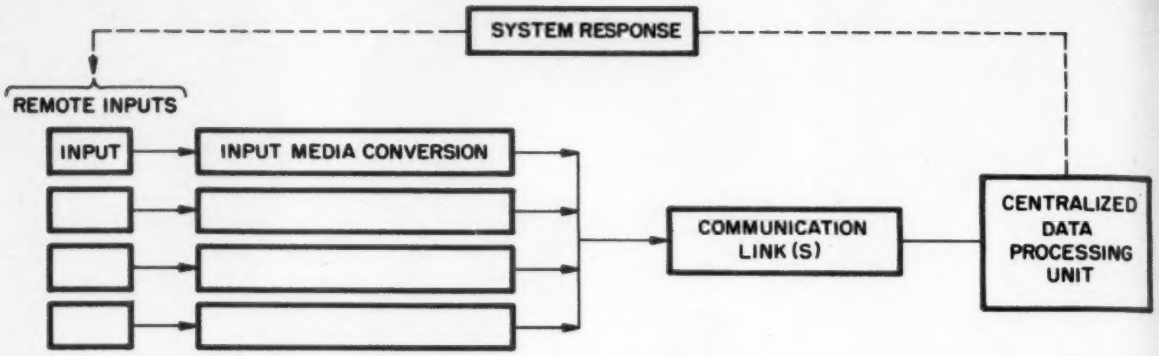


Figure 1. Real time centralized data processing—A generalized system

teller-initiated transaction inquiry on a real-time basis. Where withdrawals are involved, a positive response, i.e., "go," confirms that the balance is adequate. On demand, the system also provides detailed balance information, i.e., current value of positive assets.

3. A data processing center maintains and updates subsidiary ledger files for all member banks.

4. Non-monetary transactions originating at participant banks update subsidiary ledger files at the data processing center on a non-real-time basis.

5. On a daily basis, the data processing center provides to each bank, as required, a daily journal activity, an up-to-date general ledger posting, and a trial balance for that bank.

6. The data processing center maintains, in chronological order, a record of transactions per member bank for a period of time consistent with banking regulations. On a non-real-time basis, access to this information is available to the responsible bank, its authorized representatives, and the commissioner of the banks.

Automatic Banking System

A centralized data processing center (Figure 2) is established consisting in part of both a general purpose data processing computer and a random-access memory. The information contained within the latter is available on a real-time basis. Stored in this memory are the abbreviated pertinent data, reflecting the status of each savings account to be accommodated. For the purpose of this discussion it can be assumed that, in the aggregate, this data comprises pertinent data for all savings accounts for each participant bank.

A communication interface unit is installed in each participating bank and suitable modifications are made in each posting machine to effect an electrical entry into this unit. Telephone communication channels are employed to remote-connect the unit to the random-access memory at the data processing center.

With one variation, operation of the posting machine can proceed normally as currently performed. At the discretion of the participant banks, passbooks can be replaced by identification cards, indicating both the customer's account number and samples of acceptable signatures. Where identification cards are used, the verification of an account's ability to accommodate a withdrawal is performed in its entirety at the data processing center. Periodic statements as now employed for regular checking accounts can be used to inform customers of current account status.

In those banks electing to retain passbooks, where reference to the passbook balance is an optional prerequisite to a posting operation, independent bank philosophy dictates whether or not the balance as indicated on a customer's passbook is required to coincide with the balance of this account as reported by the data processing center prior to the completion of a given transaction. Suitable signal lights at the posting machine are used to give a "go no-go" indication to the teller of the status and confirm the validity of the proposed transaction. Upon "transaction completion" as activated at the posting machine, suitable changes are made in the central file account to ensure that it reflects "current status."

A transaction file record is maintained for authenticating account changes, zero-balancing account data at the end of the prescribed intervals, and periodically updating the extended master files comprising the ledger accounts of the participant banks. Since normal operation of the posting machine continues, a locally generated paper record is used as a further verification of the validity of the centralized transaction-file data.

Appropriate timing and bank scanning equipment are employed to ensure a minimum delay, compatible with both average and anticipated high-traffic conditions. The typical average time for the system to complete a passbook transaction is sufficiently small to be considered negligible (less than ten seconds). Under heaviest traffic conditions, i.e., when all posting machines at all banks are in operation, the customer should not experience a system delay much in excess of one-half a minute.

Mortgage-loan records for the participant banks are also maintained at the data processing center on a non-real-time basis. The existing communication channels,

when not in demand for savings account operations, are used to transmit mortgage transaction entries received at the cognizant bank. Entries submitted by mail are designated for direct delivery and subsequent handling at the data processing center.

The significant breakdown of a mortgage-loan payment into proportionate areas of principal, interest, taxes, etc., has significance only at widely separated intervals. To optimize the operation of the system, the participant banks can elect to verify to the mortgagee in terms only of total payment as received. The breakdown of this payment is handled as part of the central data processing function. Annual statements (more frequent, if the requirements are found to exist) are generated for the information of mortgagees; viz., prior to annual tax due dates.

System Operation

The system is useful in the areas of deposit accounting and mortgage-loan accounting. In both cases, there is the problem of maintaining records relative to a specific account and modifying such records in accordance with transactions initiated on a more or less random basis. The internal central processing operations required for such updating are not covered in this article. These are only suggested by the accompanying flow chart (Figure 3). The sequence of events which probably occurs in the course of such transactions are described in detail.

I. Deposit Accounting

A. General

All real-time transactions are remotely initiated as a consequence of depressing appropriate keys in a particular bank's posting machine. Electronic interrogation techniques are employed to scan the status of all posting machines and to interconnect those requiring action to the data processing center on a "demand" basis. Appropriate information flow is initiated in both directions as a consequence of recognizing the "demand" signal and subsequent transaction analysis at the data processing center.

B. Sequence Details

1. The depositor's account number, the dollar amount, and transaction type code are inserted into the system by depressing appropriate posting machine keys and a "demand" key.
2. The posting machine scanning switch (a scanning switch which sequentially samples and interrogates stations corresponding to contributing data sources) stops at the contact allocated for the given posting machine. A "ready" signal is then transmitted via a related regional center and an associated bank scanning switch to the data processing center.
3. The system scanning switch scans contributing regional centers and locks to the "ready" posting machine. A transmit signal initiated by the center itself effects the transfer of the specific account data under consideration to the data processing center computer for temporary storage and processing.
4. Reference is made to the random-access memory via the computer and the account in question is interrogated and updated. Where the transaction initiated is compatible with the current state of the account balance, the operation is concluded by the transmission of a "go" signal. Where the balance indicated is not compatible (a situation which could occur only if withdrawal is being initiated), completion of the transaction is inhibited; a "no-go" signal is transmitted to the posting machine. Note that a "go" signal frees the depressed keys and thereby signals their readiness to accept additional data. A "no-go" signal does not release the keys; however, in either case, the system is released from the posting machine.

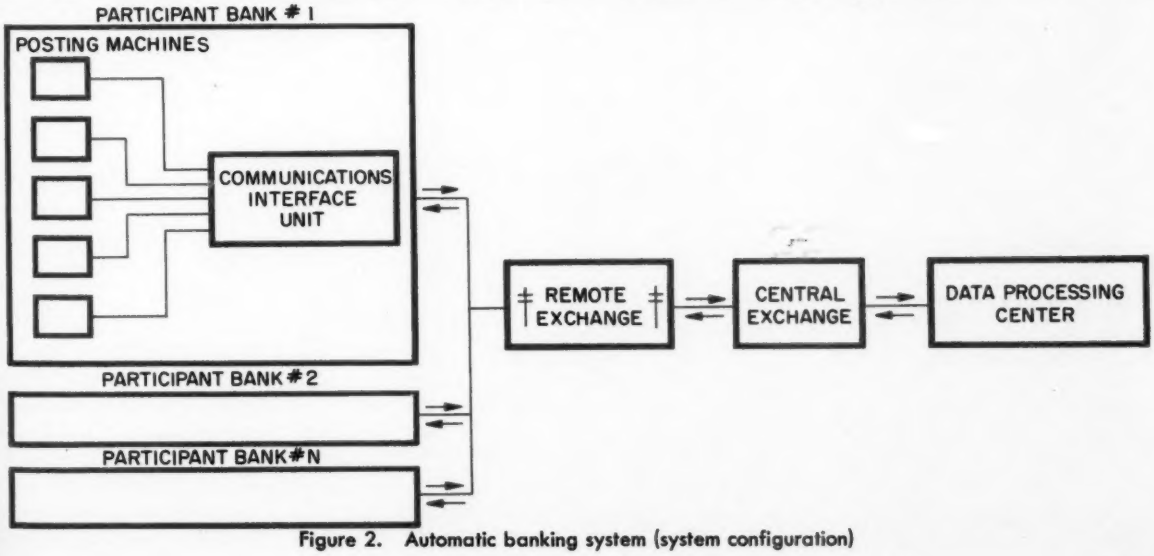


Figure 2. Automatic banking system (system configuration)

5. The "go no-go" signals are suitably displayed visually, in addition to being used for activating pre-set posting machine operations. In view of the compatibility of the system with conventional posting machines, a posting machine journal can be generated locally as a consequence of each transaction initiated. This can be used to prove out a teller's cash position at the close of each business day.
6. In the event of a "no-go" signal, an independent circuit is available and affords the teller-operator the option of communicating with the data processing center for access to more quantitative information.
7. A transaction record is generated and stored on magnetic tape at the data processing center with the completion of each posting operation.

II. Mortgage-Loan Accounting

To accommodate mortgage-loan transactions initiated remotely, posting machines at the participant banks can be employed in a manner similar to their use in deposit accounting. In view of the absence of the requirement for a real-time response, however, each participant bank can batch and schedule the transmission of mortgage-loan transactions independently. Thus, traffic load peaks are reduced, slack periods filled in, and more equitable distribution of tele-traffic enjoyed.

System Advantages

As a consequence of introducing this type of a system to serve the needs of an aggregate of savings banks, present-day banking techniques are modified, and preliminary data processing is established on a real-time basis. The following are some of the dividends and accomplishments which such a system provides.

1. Improved customer relationship by decreasing the waiting time at the teller's window and improving reliability and efficiency during high-traffic load conditions;
2. Increased teller efficiency and the ability of a given-size staff to handle more customers per unit time than is now practicable;
3. The unification of all branches of any bank via the data processing center, providing to customers rapid equivalent service in any branch;
4. The conservation of high-rental floor space dedicated to file storage at the banking office;
5. The rapid access to pertinent information by cognizant bank officials. This information might be pertinent to one account or to the entire bank's operation;
6. A significant decrease in the human-error factor by programmed and built-in operational checks;
7. The provision for optimum audit facilities, which are centralized and on-demand for all participant banks.

The benefits described above, while phrased in the terminology of the banking profession, are equivalent to those which would be realized when establishing such systems for other areas. We may conclude that similar benefits would be available and could probably be forecast in any field of activity which makes use of a rigorous system design and incorporates centralized data processing and a real-time access for systems operation.

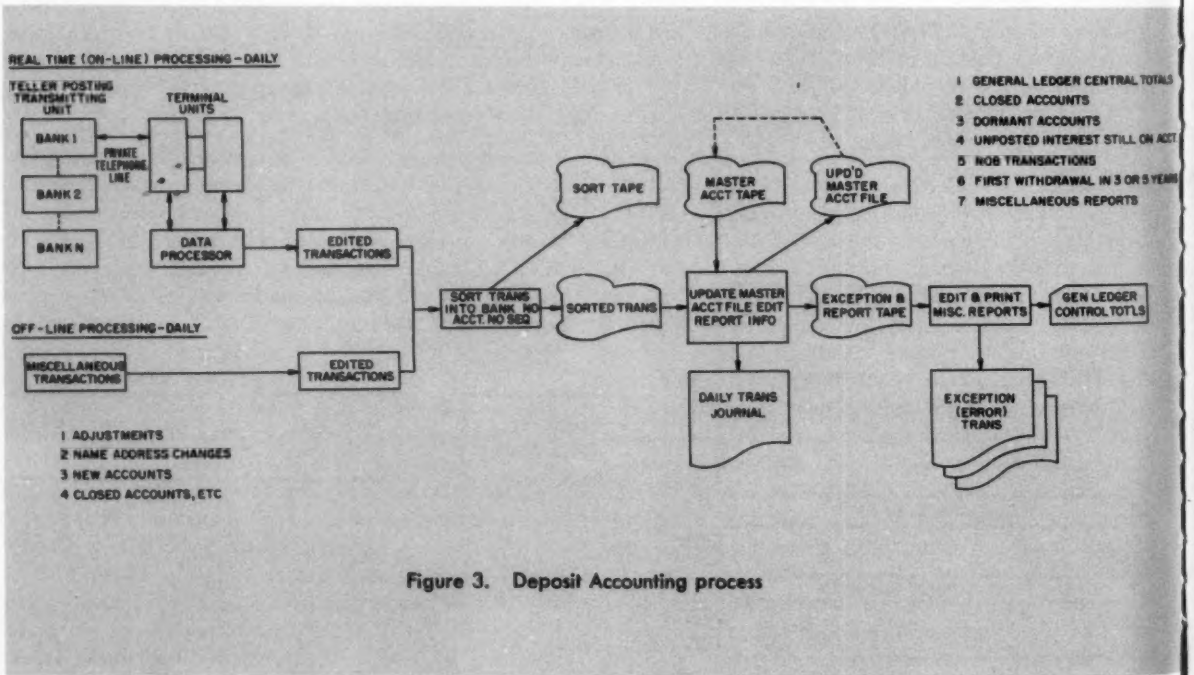
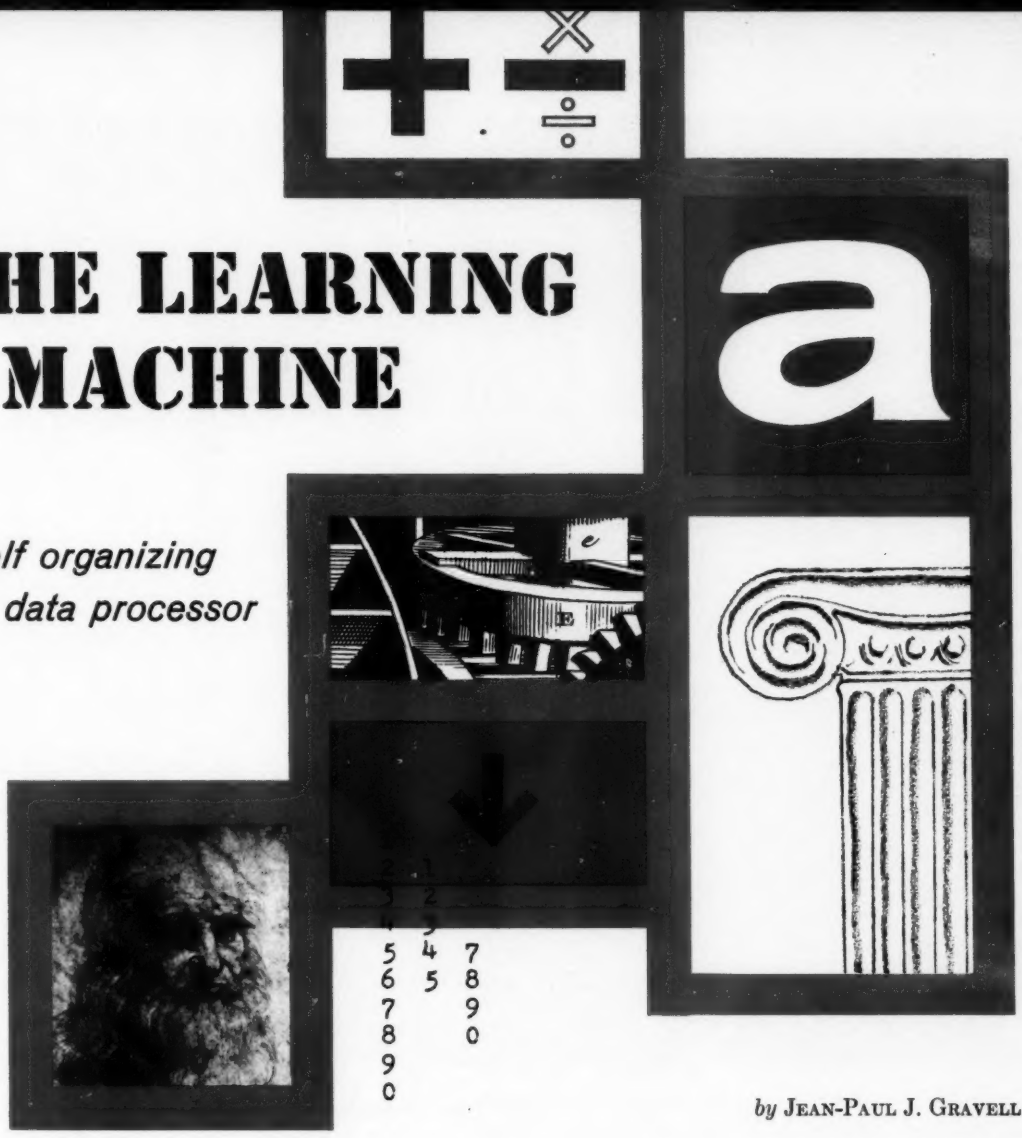


Figure 3. Deposit Accounting process

THE LEARNING MACHINE

a self organizing data processor



by JEAN-PAUL J. GRAVELL

THE STUDY of the learning or reasoning mechanism in man is an essential factor if a machine which duplicates these faculties is to be created. We know that the mental process in man is a result of an extensive interconnection of neurons in the brain. The individual neuron structure would seem to be relatively simple, but the interconnection of these neurons is accomplished in a manner that has defied all analytical attempts. The fact that a simple building block is used repetitively for the process implies that a machine could be made of fairly simple elements interconnected so as to achieve a larger purpose.

The study and development of a new class of machines, which are based on today's computer technology, but which will literally "think for themselves" is going on throughout the world. Some promising preliminary results have been published in technical papers from Stanford University, Lincoln Laboratory of M.I.T., Cornell Aeronautical Laboratory, and the University College in England, among others. Other work is proceeding at the Institute for Electro-Modeling, U.S.S.R., General Electric Company in Syracuse, Ohio State University, and at WADD, Wright-Patterson Air Force Base, Ohio. The various devices are receiving some limited publicity under the name of Learning Machines, Neuron Networks, Self-Adaptive Computers and Perceptrons.

Raytheon, for over a year, has been developing a device called the Cybertron in a Company-funded research program. It is fundamentally a learning and recognition device that can be taught by a human expert to perform a decision-making function.

A Learning Machine may be defined as a device which can be taught to respond in a certain way either through the nature of its design or by the aid of an expert teacher. In more formal language, a Learning

Figure 1. Raytheon Cybertron model K200

Machine is a device capable of extracting from both its experience and an appraisal of its actions with respect to these experiences, an improved ability for its future actions. The analysis by the machine may or may not be aided by the help of an expert teacher.

Learning is the process by which knowledge or a skill is acquired, a process which requires attention and direction of efforts. It is often a trial and error method. A teacher can speed up the learning process by directing the learning effort and thereby decreasing the number of trials. The Raytheon Cybertron (Figure 1) matches many of the characteristics exhibited by the human learning process. The learning process in man is known to require repetition in order to effect the storage of new principles out of sensed data. It is as if the structure is hesitant to accept any single piece of data as true unless it is repeated or cross-correlated to other equivalent data. This attribute seems quite contrary to the characteristics of a logic device, where information is either completely accepted or completely rejected.

We know that if areas of the human brain are removed or destroyed, whole sections of a person's memory will become fuzzy or clouded, but few specific memory items will be lacking. This also represents a significant deviation from the storage mechanism as found in the logic (computer) type device. The suggestion here is that the memory function needs to be "distributed" (not to be confused with normal redundancy), and is not dependent upon any specific single unit of storage. The Cybertron exhibits this type of response to memory alteration or destruction.

To automate the learning process, a machine capable of modifying its behavior through some sort of interaction with its environment is needed. To put it another way, we are looking for a self-adaptive action as a consequence of some type of external stimulus. Such a machine would be capable of acquiring knowledge or skill and applying it to some useful end. This could

cover many orders of complexity. It could be something as simple as character reading, which is limited to the recognition and interpretation of characters presented to it through some sort of sensing equipment. Or it could be a knowledge of many higher orders of magnitude, such as that in an automatic translation machine. Or its task could require a much deeper conceptual complexity, thus approaching a machine which could be called an electronic intellect.

In nature the single unifying process for organizing sensed data is survival. Survival is represented and interpreted to man through the pain and pleasure senses. A similar self-guidance criterion could be built into a machine which has an extensive memory function capable of storing vast amounts of data as accumulated or derived from sensory equipments. Thus the machine must operate within its environment by correlating new sensed data against previously recorded memory data and take action as a result of this correlation to optimize its survival possibilities. This should not be interpreted as implying that the actions will always optimize survival, only that they are intended to.

The method of correlation to be utilized in the machine represents one of the major difficulties in specifying the proper mode of the operation. Rather than design survival optimizing equipment, we choose to initially create a mechanism that can be taught according to the criteria of an outside agency (teacher).

Man has always endeavored to find methods of increasing his knowledge and relieving his labors without sacrificing achievements already attained. He has made great strides by inventing machines which perform, aid and supplant his mental and physical labors. The most advanced concept of this type machine in use today is the computer, which greatly speeds up the logical processing of problem solving and alleviates the drudgery of computational tasks. Many persons in various fields have considered the mechanization of some of the mental processes of man, which are either outside the domain of logic or yield to the mathematical approach only by application of enormous quantities of analysis, categorization and logical synthesis. Logical operations require a concise knowledge of the step-by-step procedure, either on a direct path or through the use of an iterative routine, by means of which a problem is solved. Such problems as inventory control, industrial automation, traffic control studies, and a host of other technical problems are now solved by the logical process which involves knowing in *advance* each and every logical step and substep in the complete solution of the problem.

There are many problems, however, which are solved only with great difficulty by logical techniques or as pointed out by Godel do not permit a solution by logic. In these areas the Learning Machine can greatly ease the difficulty of arriving at a problem solution. In addition, it can greatly simplify the solution of some of the problems now solved by other means.

The necessary parts of a simple learning element which could be used as a building block for more complex learning machines are: 1) a memory to store the essence of the data which the machine receives, 2) an association unit which combines the memory and input signals and, 3) a decision element which will act on the result achieved by the association units. Figure 2 is a block diagram of a simple learning element. The memory is modified by the action of the teacher who pushes the memory modification button whenever, in his opinion, the decision is incorrect. The decision element may, for specific applications, have a fixed or variable threshold as a reference for its action.

This device has wide applications and can be specifically applied to many military and commercial problems. For example, operators now being used to classify sonar returns for differentiating ships, whales, and schools of fish or to classify grades of apples may be released for better use of their skills by low cost, highly reliable, and efficient mechanisms. The Cybertron is quite useful in arriving at a mechanized solution to those problems in which normal human judgment and feeling enters into the derivation of a final result. The following example, which was chosen to illustrate the principle and not to be considered as an actual application demonstrates this.

In an apple-sorting problem, the machine would be taught in much the same way as the neophyte apple sorter just hired. Figure 3 shows the configuration of the device. The apples pass by the scanners on a moving belt where the data as to redness, softness, size, etc., are transformed to electrical signals which are fed into an invariance equipment (whose function is to do some pre-processing or arranging of the signals). The invariance equipment is used, where possible, to lessen the data handling load of the Cybertron. The apples are

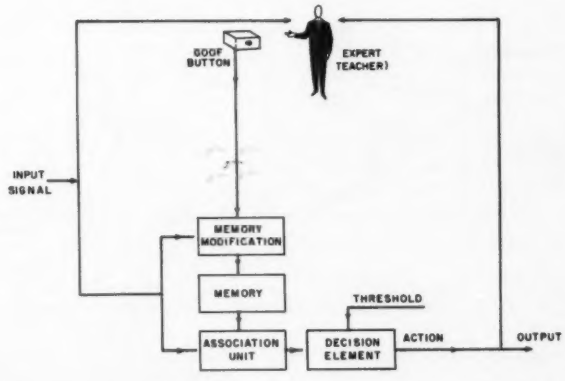
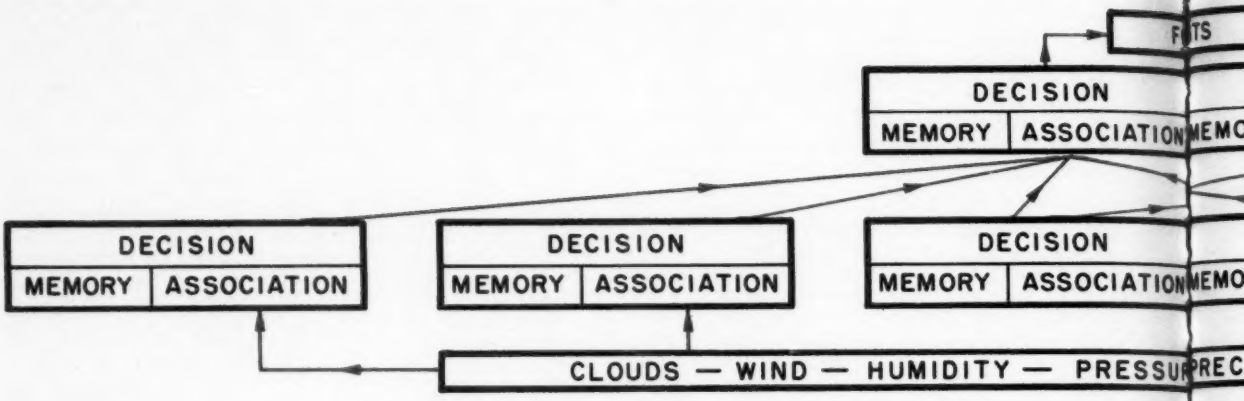


Figure 2. A simple learning element

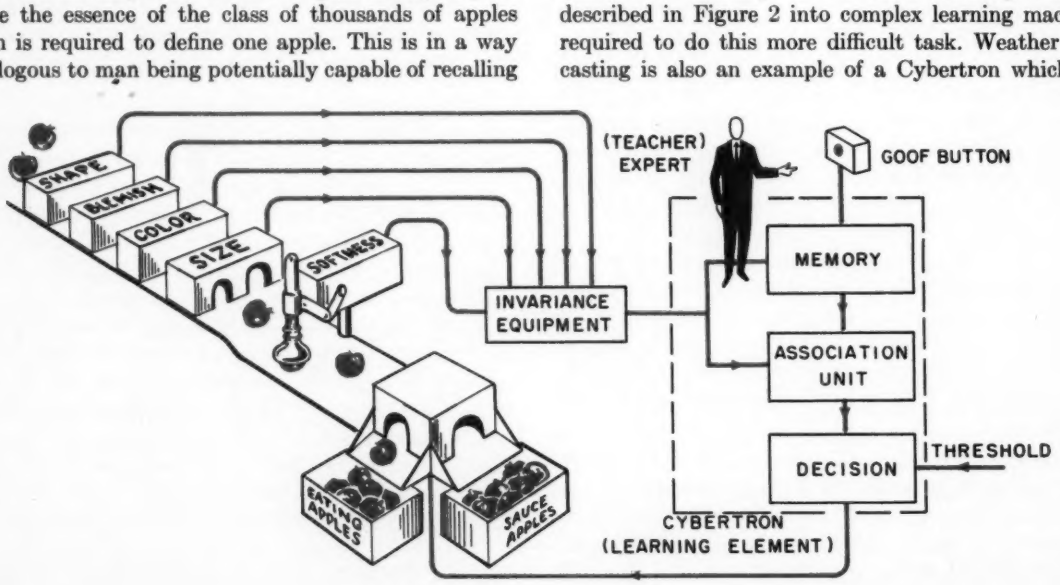


to be sorted into those for eating and those for apple sauce. As each apple is scanned, the Learning Machine takes action and dumps it either into the "eating" or "sauce" bins. An expert apple sorter in this case is overseeing the operation. Every time the machine makes a mistake he presses the "goof button" and the machine modifies its memory to take that fact into consideration and correct its future actions. After each error, the machine gets a little better at sorting apples. It is storing in its memory the essence of the difference between eating and sauce apples. It does this automatically not by storing all the data about each of the apples but by selectively picking pertinent essences of each class. The data stored in the memory is processed in the association unit along with the incoming signals and a decision is made which triggers an action.

A fundamentally important facet of the device is that the memory need be of no greater capacity to store the essence of the class of thousands of apples than is required to define one apple. This is in a way analogous to man being potentially capable of recalling nearly all of the significant concepts connected with his experience but not by recalling all superfluous sensed signals unconnected with any specific new information or experience. This suggests that the memory function within man does not consist of separate memory cells capable of recording every item in a landscape viewed (i. e., millions of bits per scene), but rather is an accumulation of concepts and relationships stored in his mind so that only significant items are retained.

Another important feature is the fact that after a machine has learned its assigned task its memory may be copied and transferred to a simpler machine called an AIDE (Adapted Identification Decision Equipment) which is capable of performing the task but cannot do any further learning. AIDE is much simpler in design and smaller and more compact.

Some tasks such as weather forecasting will require connection of many of the basic learning elements described in Figure 2 into complex learning machines required to do this more difficult task. Weather forecasting is also an example of a Cybertron which can



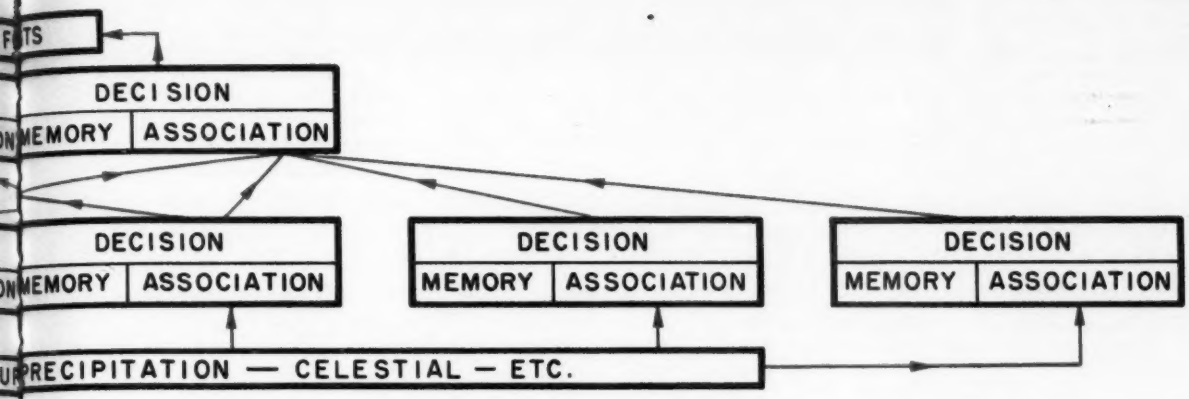


Figure 4. Weather forecasting Cybertron

literally teach itself without the aid of the outside expert by comparing its forecasts with the results and automatically correcting its errors by improving its capabilities. Figure 4 is a simplified diagram for a possible Weather Forecasting Cybertron which is made up of many of the simple learning elements.

Both the Cybertron and AIDE will undoubtedly make important contributions to the economic solution of problems in the areas of general recognition tasks such as those involved in quality control, intelligence data analysis, IFF analysis, and handwriting recognition; general sorting tasks, such as parts or component grading; and signal analysis, such as hand-transmitted Morse code identification.

Some of the other proposed uses for the Cybertron and AIDE are in the fields of anti-submarine and anti-missile warfare for the detection and recognition of the target from radar or sonar data.

At present, Raytheon has many aspects of this new field under consideration. Simulation of a simple Cybertron has been carried out on a large general purpose digital computer. Two Learning Machines have been constructed and are being actively used in the Advanced Development Laboratory of Raytheon's Communications and Data Processing Operations. The smaller of the machines, the K100, is actively working on problems from data supplied by the Air Force, Signal Corps and Navy. These problems deal with the sorting of signals for doing recognitions. This single learning element uses punched paper tape as an input-output medium and a high speed digital-arithmetic-association unit. Cybertron K200 of Figure 1 is a much larger Learning Machine designed to recognize and type out speech sounds. Its input is a microphone and its output is a Flexowriter electric typewriter. It has the capability of recognizing and typing out all the typical American word sounds by using its 192 learning elements.

In summing up we can see that the Learning Machine is a new class of device that does not require detailed knowledge of the method of problem solution. It obtains the solution by forming its own concept of the problem through an auto-adaptive process which results in automatic modification of its memory and behavior as it is exposed to an environment. Through the technique of automatic progressive categorization of the information received, a simple Learning Machine can be used to solve many problems, be it a simple task of reading block print or the more advanced task of recognizing vocal sounds. For the more complex tasks, or for more rapid learning of simpler tasks, groups of simple learning elements can be interconnected into a complex Learning Machine. Such a learning device is capable of categorizing and forming subcategories within major categories and can be taught to recognize objects, situations, or concepts. The device can learn, and the organization of its memory to the task, by a correlation technique analagous to a Gauss-Seidel iteration procedure, is convergent.

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BONUS PAYMENTS for patent disclosures were received by:

E. Adler	Speed up of Avalanche Transistor Switch Recovery Time
Robert Anderson	Cross Guide Coupler
Donald S. Banks	Radar Scanning
W. G. Beauregard	Parametric Amplifier
W. G. Beauregard	Diplexer Multiplexer
Leonard Bjork	Transition from Coaxial Transmission Line to Interdigital Delay Line
Frank Blitzer	Gyrometer
Geoffrey J. Bonelle	Antenna Array
Colin Bowness	Circular Polarized TEM Device in TEM Structure
Colin Bowness	Microwave Ferrite Element
Colin Bowness	A Non-Reciprocal Amplitron Circuit
Merle H. Boyd	Cascade Coolant Flow for M-BWO
Anthony J. Caggiono	Fabrication of Transistors Using Evaporated Base, Alloyed Emitter Technique
Harry F. Chapell	Transition from Coaxial Transmission Line to Interdigital Delay Line
R. M. Chute	Ship's Past Position Indicator
Mikael Ciftan	Optical Maser with Mode Selection
Peter Fowler	Accelerometer Design
Francis A. Gicca	Navigation System
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William T. Maloney	Five-Frequency Parametric Down-Converter
Russell T. Mannette	Cascade Coolant Flow for M-BWO
James C. McKalip, Jr.	Saturating Logic Inverters with Avalanche Turn-On
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Matthew S. Miller	Power Divider
John Q. Owen	Microwave Ferrite Element
John Q. Owen	A Non-Reciprocal Amplitron Circuit
Ernst Schloemann	Parametric Amplifier
Clinton G. Shafer	Parametric Amplifier
H. J. Tracy	Non-Conductive Filter Liner
George R. Welti	Hash-Canceling Pulse Compression Radar System
Douglas M. Warschauer	Use of Impurity and Trap Doping for Electrical Isolation, Introduction of Delay or Phase Shift, and Suggestion for Device
John Zorzy	Tunnel Diode Augmenter

PATENTS

PATENTS ISSUED to Raytheon during the months of January and February, 1961 include:*

U.S. Patent No.	*Inventor*	*Title*
2,967,264	E. C. Dench	Grid-Controlled Magnetrons
2,969,458	G. B. Parkinson	Anti-Image Systems
2,969,487	F. J. Bourassa	Sealed Crystal Diode Packages
2,970,213	F. M. Dukat	Hybrid Radio Receiving Circuits
2,970,264	W. T. Eriksen	Elapsed Time Indicators
2,970,276	K. Dollinger	Noise Reduction Systems
2,970,294	S. S. Guterman	Magnetic Control Circuits for Shift Registers
2,971,049	H. Zucker	Synchronous Demodulator for Color Receivers
2,971,112	E. C. Dench	Traveling Wave Tube Electrode Mountings
2,971,121	E. C. Dench	Magnetron Amplifiers
2,971,169	P. A. Sullivan	Pulse Position Modulation Systems
2,972,731	J. N. Beebe	Echo Distance Measuring Systems

*Any person wishing to obtain copies of these patents should contact his library.

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PAPERS & PUBLICATIONS

Beginning with this issue of ELECTRONIC PROGRESS, all papers which have been presented at scientific meetings and published in technical journals will be listed in this section. In order to ensure completeness in future issues, authors are requested to advise the Secretary, Technical Publications Panel (Lexington X240) when papers are accepted for presentation and publication.

Papers Presented at Scientific Meetings

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